bq24187 2A, 30V Host-Controlled Single-Input, Single Cell Switchmode Li-Ion Battery Charger with Integrated Sense Element and 1A USB-OTG Support

1 Features

- Charge Time Optimizer (Enhanced CC/CV Transition) for Faster Charging
- Integrated FETs for Up to 2A Charge Rate at 5% Accuracy and 93% Peak Efficiency
- Boost Capability to Supply 5V at 1A at IN for USB OTG Supply
- Integrated Current Sense Resistor for Smallest Size and Cost
- 30V Input Rating with Over-Voltage Protection Supports 5V USB2.0/3.0 with 6.5V OVP
- Small Solution Size In a 2,4mm x 2,4mm 36-ball WCSP or 4mm x 4mm QFN-24 Package
- Safe and Accurate Battery Management Functions Programmed Using I^2C Interface
  - Charge Voltage, Current, Termination Threshold, Input Current Limit, V_{IN_DPM} Threshold
  - Voltage-based, JEITA Compatible NTC Monitoring Input
  - Thermal Regulation Protection for Input Current Control
  - Thermal Shutdown and Protection

2 Applications

- Smartphones and Tablets
- Handheld Products
- Power Banks and External Battery Packs
- Small Power Tools
- Portable Media Players and Gaming

3 Description

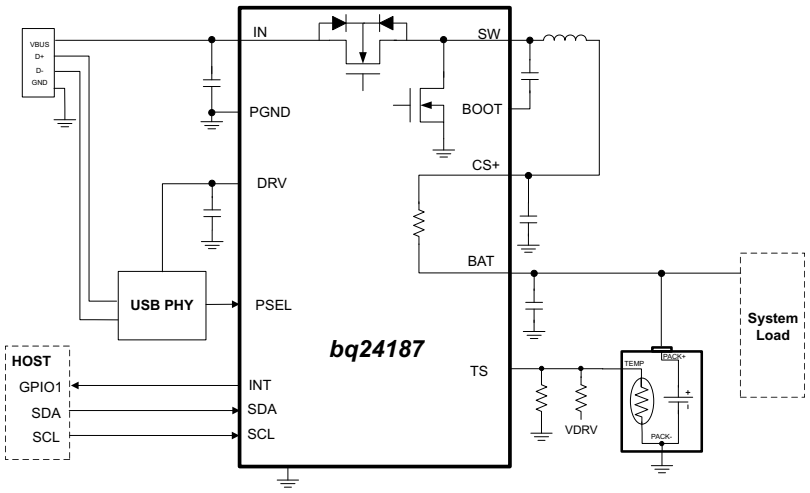
The bq24187 is a highly integrated single cell Li-Ion battery charger targeted for space-limited, portable applications with high capacity batteries. The single cell charger has a single input that supports operation from either a USB port or wall adapter supply for a versatile solution. The integrated sense element reduces solution size and external component count. The charge parameters are programmable using the I2C interface. To Support USB OTG applications, the bq24187 is configurable to boost the battery voltage to 5V at the input. In this mode, the bq24187 supplies up to 1A and operates with battery voltages down to 3.3V. A voltage-based, JEITA compatible battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safe charging.

Device Information

ORDER NUMBER(1)	PACKAGE	BODY SIZE
bq24187YFFR	DSBGA (36)	2,4mm × 2,4mm
bq24187RGER(2)	VQFN (24)	4mm × 4mm

(1) For ordering information see the addendums at the end of the data sheet.
(2) PREVIEW

4 Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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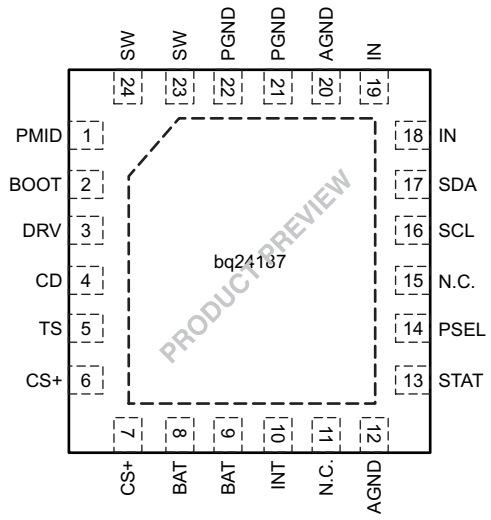
5 Revision History

DATE	REVISION	NOTES
April 2014	*	Initial release.

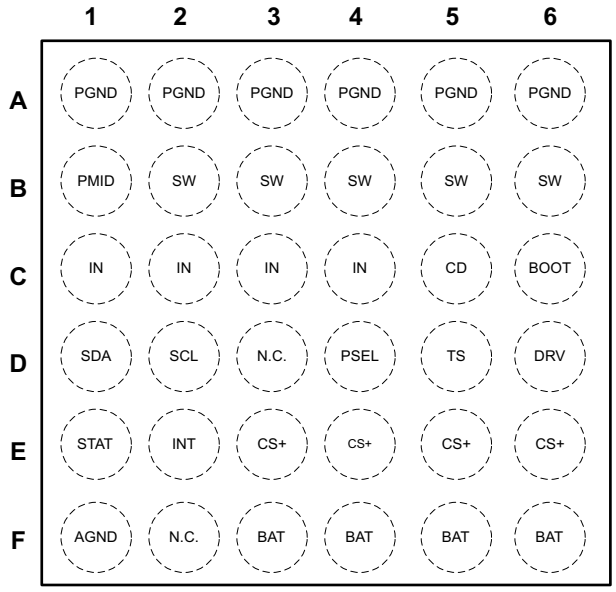
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6 Terminal Configuration and Functions

RGE Package
(24-Terminal 4 mm X 4 mm QFN)
Top View



YFF Package
(36-Ball 2,6 mm X 2,6 mm DSBGA)
Top View



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	YFF	RGE		
AGND	F1	12, 20		Analog Ground. Connect to the PGND TERMINALs and the ground plane of the circuit.
BAT	F3-F6	8, 9	I/O	Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT to GND with a 1µF capacitor.
BOOT	C6	2	I	High Side MOSFET Gate Driver Supply. Connect a 0.033µF ceramic capacitor (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
CD	C5	4	I	IC Hardware Disable Input. Drive CD high to place the bq24187 in Hi-Z mode. Drive CD low for normal operation.

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Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	YFF	RGE		
DRV	D6	3	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. Bypass DRV to PGND with a 1µF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $V_{IN} > V_{UVLO}$ and $V_{IN} > (V_{BAT} + V_{SLP})$.
IN	C1-C4	18, 19	I	DC Input Power Supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to PGND with at least a 4.7µF ceramic capacitor.
INT	E2	10	O	Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. INT is enabled /disabled using the EN_STAT bit in the control register. Connect INT to a logic rail through a 100kΩ resistor to communicate with the host processor.
N.C.	D3, F2	11, 15	--	Connect to the ground plane of the circuit.
PGND	A1-A6	21, 22	--	Ground terminal. Connect to the the ground plane of the circuit.
PMID	B1	1	I	High Side Bypass Connection. Connect a 1µF capacitor from PMID to PGND as close to the PMID and PGND TERMINALs as possible.
PSEL	D4	14	I	Hardware Input Current Limit. In DEFAULT mode, PSEL selects the input current limit during DEFAULT mode. Drive PSEL high to select USB100 mode, drive PSEL low to select 1.5A mode.
SCL	D2	16	I	I^2C Interface Clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	D1	17	I/O	I^2C Interface Data. Connect SDA to the logic rail through a 10kΩ resistor.
STAT	E1	13	O	Status Output. STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. STAT is enabled /disabled using the EN_STAT bit in the control register. Connect STAT to a logic rail using an LED for visual indication or through a 10kΩ resistor to communicate with the host processor.
SW	B2-B6	23, 24	O	Inductor Connection. Connect to the switched side of the external inductor.
CS+	E3-E6	6, 7	I	System Voltage Sense and Charger FET Connection. Connect CS+ to the inductor. Bypass CS+ locally with 20µF.
TS	D5	5	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA compatibility. TS faults are reported by the I^2C interface. Pull TS high to V_{DRV} to disable the TS function. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
Thermal PAD	–	–	–	There is an internal electrical connection between the exposed thermal pad and the PGND TERMINAL of the device. The thermal pad must be connected to the same potential as the PGND TERMINAL on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. PGND TERMINAL must be connected to ground at all times.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Terminal voltage range (with respect to PGND)	IN	–1.3	30	V
	BOOT	–0.3	30	V
	SW	–0.7	20	V
	SDA, SCL, CS+, BAT, STAT, DRV, TS, PSEL, INT	–0.3	5	V
BOOT to SW		–0.3	5	V
Output Current (Continuous)	SW		4.5	A
	CS+, BAT (charging)		3.5	A
Input Current (Continuous)			2.75	A
Output Sink Current	STAT, INT		10	mA
Operating free-air temperature range		–40	85	°C
Junction temperature, T_J		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	–65	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	IN voltage	4.2	28(1)	V
	IN operating voltage	4.2	6.0	
I_{IN}	Input current, IN input		2.5	A
I_{SW}	Ouput Current from SW, DC		2	A
I_{BAT}	Charge Current		2	A
T_J	Operating junction temperature, T_J	0	125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOST or SW terminals. A *tight* layout minimizes switching noise.

7.4 Thermal Information

THERMAL METRIC(1)		bq24187		UNIT
		YFF	RGE	
		36 TERMINALS	24 TERMINALS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.8	32.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.5	30.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	10	3.3	
ψ_{JT}	Junction-to-top characterization parameter	2.6	0.4	
ψ_{JB}	Junction-to-board characterization parameter	9.9	9.3	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Circuit of Figure 6, $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = –40°C–125°C and T_J=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENTS							
I_{IN}	Supply current for control	$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, PWM switching			15		mA
		$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, PWM NOT switching				6.5	
		0°C< T_J < 85°C, V_{IN} = 5V, High-Z Mode				250	µA
I_{BAT_HIZ}	Battery discharge current in high impedance mode, (BAT, SW, CS+)	0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 5V, SCL, SDA = 0V or 1.8V, High-Z Mode				15	µA
		0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 0V, SCL, SDA = 0V or 1.8V				80	µA
CHARGER PARAMETERS							
R_{SENSE}	Internal Sense Element Resistance	Measured from BAT to CS+, V_{BAT} = 4.2V, High-Z mode	YFF		17	25	mΩ
			RGE		32	47	mΩ
V_{BATREG}	Charge voltage	Operating in voltage regulation, Programmable range		3.5		4.44	V
	Voltage Regulation Accuracy	T_J = 25°C, RGE Package		–0.5%		0.5%	
		T_J = 0°C to 85°C, RGE and YFF Package		–0.75%		0.75%	
		T_J = 0°C to 125°C, RGE and YFF Package		-1.0%		1.0%	
I_{CHARGE}	Fast charge current range	$V_{LOWV} \le V_{BAT} < V_{BAT(REG)}$		500		2000	mA
	Fast charge current accuracy	500 mA ≤ I_{CHARGE} ≤ 1A		–10%		10%	
		I_{CHARGE} ≥ 1000mA		–5%		5%	
$V_{BATSHRT}$	Battery short circuit threshold			1.9	2	2.1	V
$V_{BATSHRT(hys)}$	Hysteresis for V_{LOWV}	Battery voltage falling			100		mV
$I_{BATSHRT}$	Battery short circuit charge current	$V_{BAT} < V_{LOWV}$		33.5	50	66.5	mA
I_{TERM}	Termination charge current	$_{ITERM}$ ≤ 50mA		–30%		30%	
		50mA < I_{TERM} < 200mA		–15%		15%	
		I_{TERM} ≥ 200mA		–15%		10%	
V_{RCH}	Recharge threshold voltage	Below V_{OREG}		100	120	150	mV
$V_{DET(SRC1)}$	Battery detection voltage threshold (TE = 1)	During current source (Turn $I_{BATSHRT}$ off)			V_{RCH}		V
$V_{DET(SRC2)}$		During current source (Turn $I_{BATSHRT}$ on)			V_{RCH} – 200mV		
$V_{DET(SNK)}$		During current sink			$V_{BATSHRT}$		
I_{DETECT}	Battery detection current before charge done (sink current)	Termination enabled (TE = 1)			7		mA

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Electrical Characteristics (continued)

Circuit of Figure 6, $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = –40°C–125°C and T_J=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENT LIMITING							
I_{IN_USB}	Input current limiting threshold	USB charge mode, V_{IN} = 5V, Current pulled from SW	I_{INLIM} = USB100	90	95	100	mA
			I_{INLIM} = USB500	450	475	500	
			I_{INLIM} = USB150	125	140	150	
			I_{INLIJM} = USB900	800	850	900	
			I_{INLIM} = 1.5A	1425	1500	1575	
			I_{INLIM} = 2.0A	1850	2000	2200	
V_{IN_DPM}	Input based DPM threshold range	Charge mode, programmable via I^2C		4.2		4.76	V
	V_{IN_DPM} threshold Accuracy			–3%		3%	
VDRV BIAS REGULATOR							
V_{DRV}	Internal bias regulator voltage	V_{IN}>5V		4.3	4.8	5.3	V
I_{DRV}	DRV Output current			0		10	mA
V_{DO_DRV}	DRV Dropout voltage (V_{IN} – V_{DRV})	I_{IN} = 1A, V_{IN} = 4.2V, I_{DRV} = 10mA				450	mV
STATUS OUTPUT (STAT, INT)							
V_{OL}	Low-level output saturation voltage	I_O = 5 mA, sink current				0.4	V
I_{IH}	High-level leakage current	$V_{/CHG}$ = $V_{/PG}$ = 5V				1	µA
INPUT TERMINALS (CD, PSEL)							
V_{IL}	Input low threshold					0.4	V
V_{IH}	Input high threshold			1.4			V
$R_{PULLDOWN}$	CD pull-down resistance	CD only			100		kΩ
PROTECTION							
V_{UVLO}	IC active threshold voltage	V_{IN} rising		3.2	3.3	3.4	V
V_{UVLO_HYS}	IC active hysteresis	V_{IN} falling from above V_{UVLO}			300		mV
V_{SLP}	Sleep-mode entry threshold, V_{IN}-V_{BAT}	2.0 V ≤ V_{BAT} ≤ V_{BATREG}, V_{IN} falling		0	40	120	mV
V_{SLP_HYS}	Sleep-mode exit hysteresis			40	100	190	mV
V_{OVP}	Input supply OVP threshold voltage	IN rising, 100mV hysteresis		6.25	6.5	6.75	V
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge		1.03 × V_{BATREG}	1.05 × V_{BATREG}	1.07 × V_{BATREG}	V
V_{BOVP_HYS}	V_{BOVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}			1		% of V_{BATREG}
$I_{CbCLIMIT}$	Cycle-by-cycle current limit	V_{CS+} shorted		4.1	4.5	4.9	A
T_{SHTDWN}	Thermal trip				150		°C
	Thermal hysteresis				10		
T_{REG}	Thermal regulation threshold	Charge current begins to cut off			125		°C
	Safety Timer Accuracy			–20%		20%	
PWM							
R_{DSON_Q1}	Internal top MOSFET on-resistance	YFF Package: Measured from IN to SW			75	120	mΩ
		RGE Package: Measured from IN to SW			80	135	mΩ
R_{DSON_Q2}	Internal bottom N-channel MOSFET on-resistance	YFF Package: Measured from SW to PGND			75	115	mΩ
		RGE Package: Measured from SW to PGND			80	135	mΩ

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Electrical Characteristics (continued)

Circuit of Figure 6, $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = –40°C–125°C and T_J=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BATTERY-PACK NTC MONITOR							
V_{HOT}	High temperature threshold	V_{TS} falling, 2% V_{DRV} Hysteresis		27.3	30	32.6	$\%V_{DRV}$
V_{WARM}	Warm temperature threshold	V_{TS} falling, 2% V_{DRV} Hysteresis		36.0	38.3	41.2	$\%V_{DRV}$
V_{COOL}	Cool temperature threshold	V_{TS} rising, 2% V_{DRV} Hysteresis		54.7	56.4	58.1	$\%V_{DRV}$
V_{COLD}	Low temperature threshold	V_{TS} rising, 2% V_{DRV} Hysteresis		58.2	60	61.8	$\%V_{DRV}$
TSOFF	TS Disable threshold	V_{TS} rising, 4% V_{DRV} Hysteresis		80		85	$\%V_{DRV}$
I^2C COMPATIBLE INTERFACE							
V_{IH}	Input low threshold level	$V_{PULL-UP}$=1.8V, SDA and SCL		1.3			V
V_{IL}	Input low threshold level	$V_{PULL-UP}$=1.8V, SDA and SCL				0.4	V
V_{OL}	Output low threshold level	I_L=5mA, sink current				0.4	V
I_{BIAS}	High-Level leakage current	$V_{PULL-UP}$=1.8V, SDA and SCL				1	µA
OTG BOOST SUPPLY							
I_{QBAT_BOOST}	Quiescent current during boost mode (BAT TERMINAL)	2.7V<V_{BAT}<4.5V, no switching				100	µA
	Boost voltage range for specified boost operation			3.3		4.5	V
V_{IN_BOOST}	Boost output voltage (to terminal VBUS)	2.7V<V_{BAT}<4.5V over line and load		4.95	5.05	5.2	V
I_{BO}	Maximum output current for boost	2.7V<V_{BAT}<4.5V	BOOST_ILIM=1	1000			mA
			BOOST_ILIM=0	500			
I_{BLIMIT}	Cycle by cycle current limit for boost (measured at lowside FET)	2.7V<V_{BAT}<4.5V	BOOST_ILIM=1		4		A
			BOOST_ILIM=0		2		
$V_{BOOSTOVP}$	Over voltage protection threshold for boost (IN terminal)	Signals fault and exits boost mode		5.8	6	6.2	V
$V_{BURST(ENT)}$	Upper V_{IN} voltage threshold to enter burst mode (stop switching)			5.1	5.2	5.3	V
$V_{BURST(EXIT)}$	Lower V_{BUS} voltage threshold to exit burst mode (start switching)			4.9	5	5.1	V

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7.6 Timing Requirements

Circuit of Figure 6, $V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = –40°C–125°C and T_J=25ºC for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGER PARAMETERS						
	Deglitch time for battery short to fast charge transition	V_{BAT} rising or falling		1		ms
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL}=100ns		32		ms
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL}=100ns		32		ms
$t_{DETECT(SRC)}$	Battery detection time (sourcing current)	Termination enabled (TE = 1)		2		s
$t_{DETECT(SNK)}$	Battery detection time (sinking current)	Termination enabled (TE = 1)		250		ms
INPUT TERMINALS (CD, PSEL)						
	Deglitch for CD and PSEL	CD or PSEL rising/falling		100		µs
PROTECTION						
$t_{DGL(VSLP)}$	Deglitch time for supply rising above $V_{SLP}+V_{SLP_EXIT}$	Rising voltage, 2-mV over drive, t_{RISE}=100ns		30		ms
$t_{DGL(BOVP)}$	BOVP Deglitch	Battery entering/exiting BOVP		8		ms
	Safety Timer Accuracy		–20%		20%	
BATTERY-PACK NTC MONITOR						
$t_{DGL(TS)}$	Deglitch time on TS change	Applies to V_{HOT} , V_{WARM} , V_{COOL} , and V_{COLD}		50		ms
I²C COMPATIBLE INTERFACE						
$t_{WATCHDOG}$			30	50		s
$t_{I2CRESET}$				700		ms

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency		1.35	1.5	1.65	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0%			

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7.8 Typical Characteristics

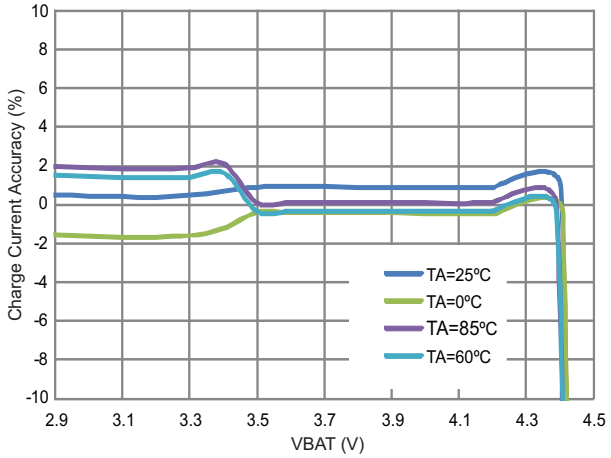


Figure 1. Current Charge vs Battery Voltage

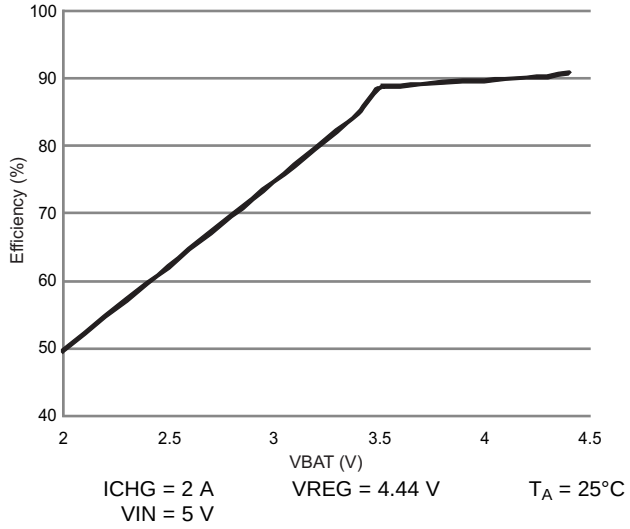


Figure 2. Efficiency vs Batter`y Charge

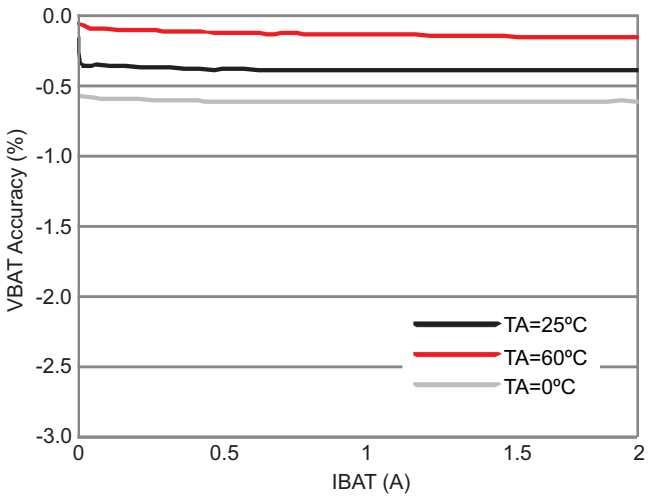


Figure 3. VBAT Accuracy vs IBAT – 4.2 V Setting

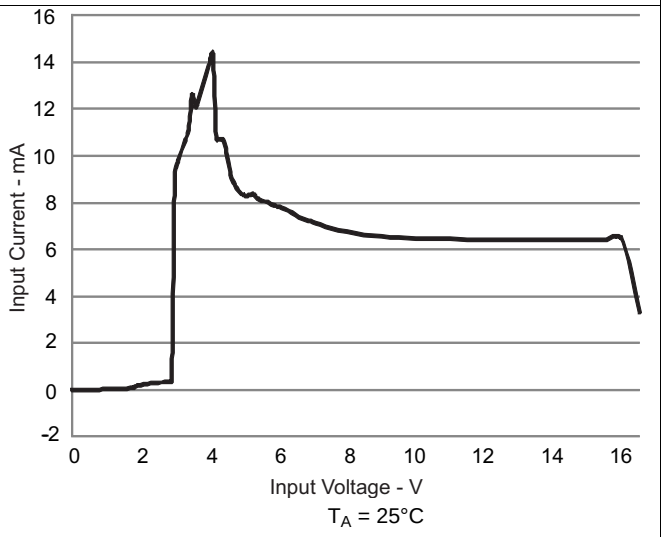


Figure 4. Input IQ - No Battery, No System

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8 Detailed Description

8.1 Overview

The bq24187 is a highly integrated single cell Li-Ion battery charger targeted for space-limited, portable applications with high capacity batteries. The single cell charger has a single input that supports operation from either a USB port or wall adapter supply for a versatile solution. The integrated sense element reduces solution size and external component count. The charge parameters are programmable using the I2C interface. To Support USB OTG applications, the bq24187 is configurable to boost the battery voltage to 5V at the input. In this mode, the bq24187 supplies up to 1A and operates with battery voltages down to 3.3V. The battery is charged in three phases: precharge, fast charge constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, a voltage-based, JEITA compatible battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safe charging.

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8.2 Functional Block Diagrams

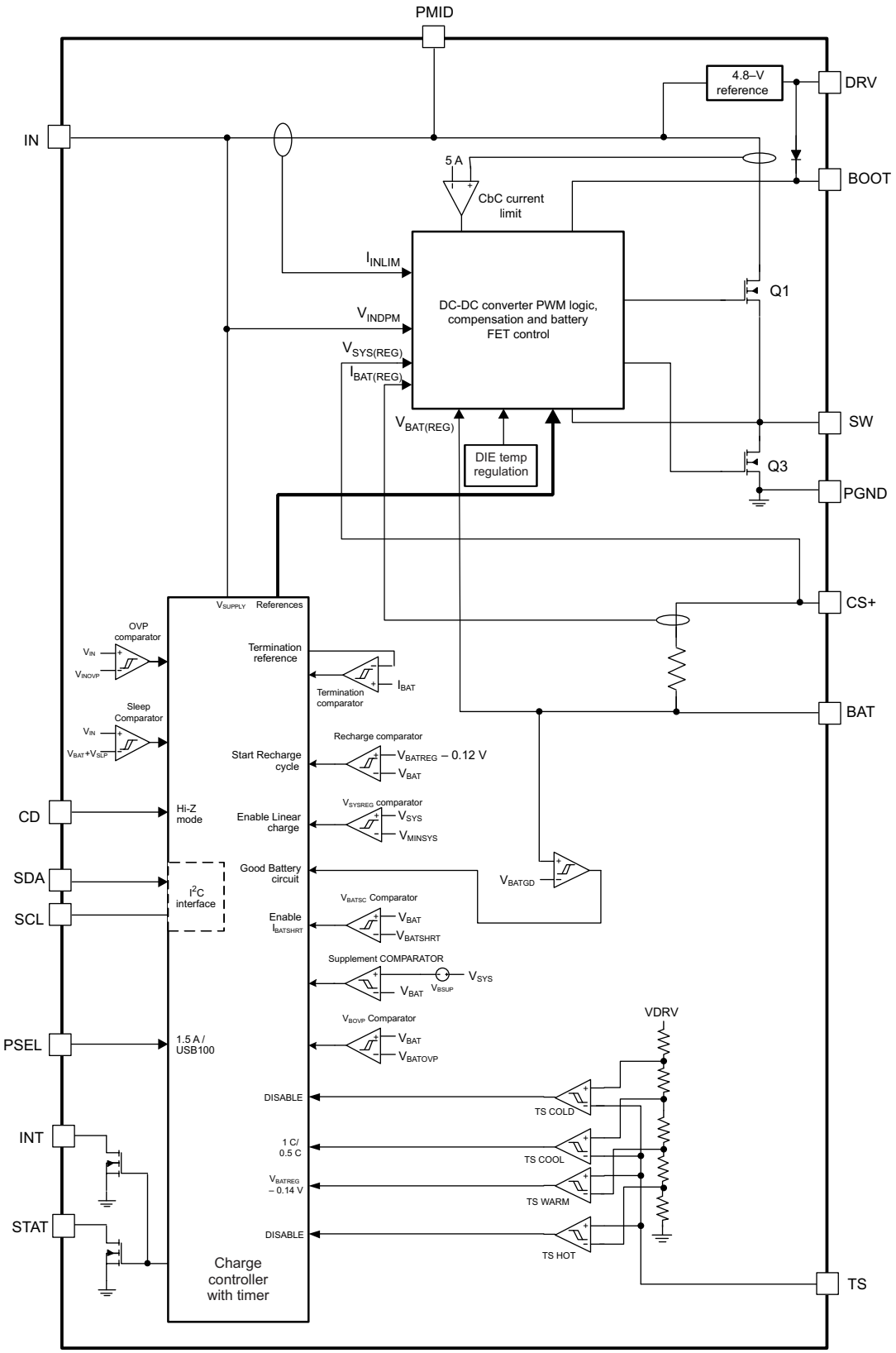


Figure 5. Block Diagram In Charging Mode

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Functional Block Diagrams (continued)

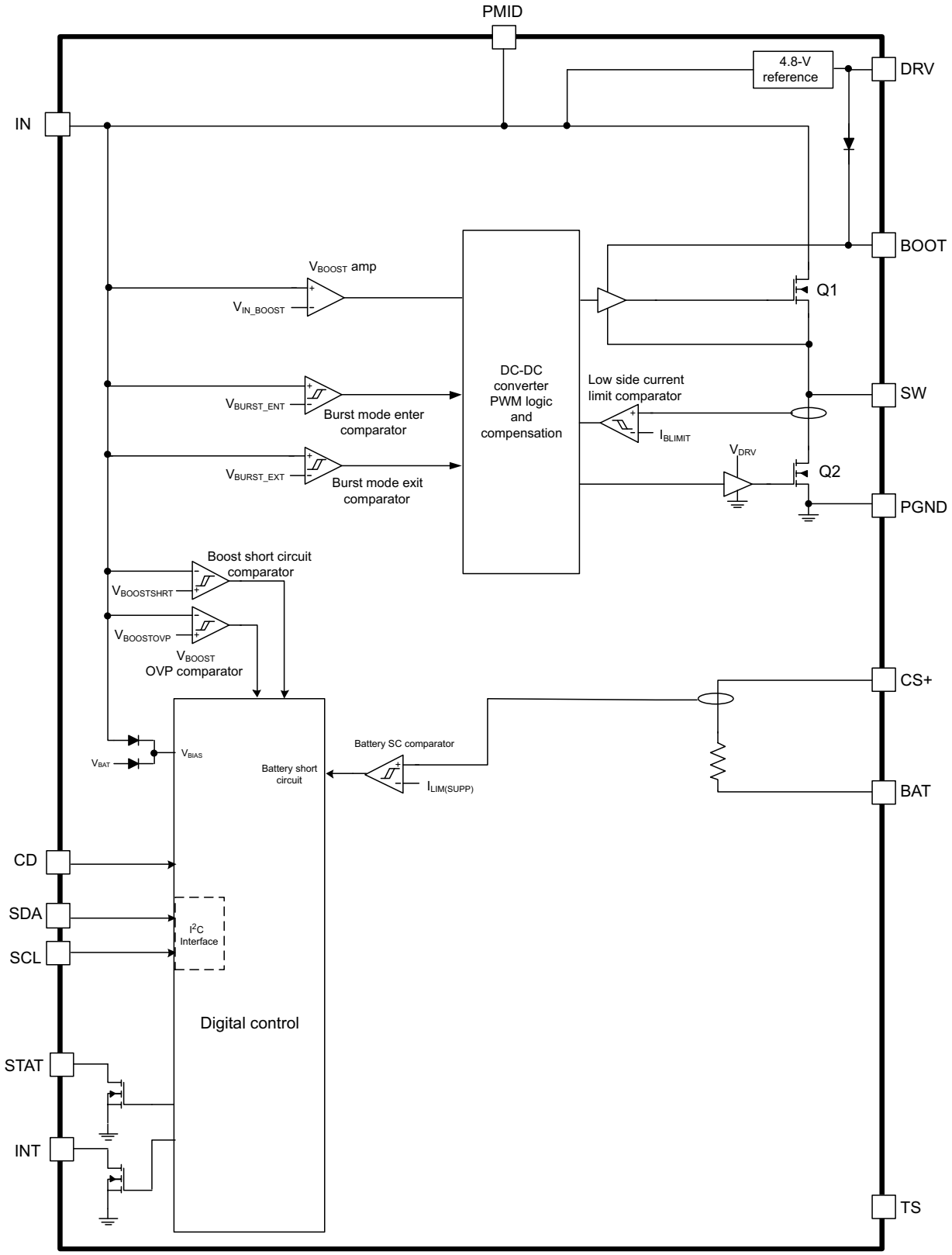


Figure 6. Block Diagram In Boost Mode

8.3 Feature Description

The bq24187 is a highly integrated single cell Li-Ion battery charger targeted for space-limited, portable applications with high capacity batteries. The single cell charger has a single input that supports operation from either a USB port or wall adapter supply for a versatile solution. The integrated sense element reduces solution size and external component count. The charge parameters are programmable using the I2C interface. To Support USB OTG applications, the bq24187 is configurable to boost the battery voltage to 5V at the input. In this mode, the bq24187 supplies up to 1A and operates with battery voltages down to 3.3V. The battery is charged in three phases: precharge, fast charge constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, a voltage-based, JEITA compatible battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safe charging.

The Device Functional Modes section explains these features in detail.

8.4 Device Functional Modes

8.4.1 High Impedance Mode (Hi-Z Mode)

High Impedance mode (Hi-Z mode) is the low quiescent current state for the bq24187. During Hi-Z mode, the buck converter is off. The bq24187 is in Hi-Z mode when $VI_N < V_{UVLO}$, the HZ_MODE bit in the I2C is '1' or the CD terminal is driven high. Hi-Z mode resets the safety timer.

The bq24187 contains a CD input that is used to disable the IC and place the bq24187 into high-impedance mode. Drive CD low to enable the bq24187 and enter normal operation. Drive CD high to disable charge and place the bq24187 into high-impedance mode. CD is internally pulled down to PGND with a 100kΩ resistor. When exiting Hi-Z mode, charging resumes in approximately 110ms.

8.4.1.1 Input Connected

8.4.1.1.1 Input Voltage Protection In Charge Mode

8.4.1.1.1.1 Sleep Mode

The bq24187 enters the low-power sleep mode if the voltage on VIN falls below sleep-mode entry threshold, $V_{BAT}+V_{SLP}$, and V_{IN} is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of V_{IN}. When $V_{IN} < V_{BAT}+ V_{SLP}$, the bq24187 turns off the PWM converter, sends a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. Once $V_{IN} > V_{BAT}+ V_{SLP}$, the STATx and FAULT_x bits are cleared and the device initiates a new charge cycle. The FAULT_x bits are not cleared until they are read in the I^2C and the sleep condition no longer exists.

8.4.1.1.1.2 Input Voltage Based DPM (V_{IN}-DPM)

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage deceases. Once the supply drops to V_{IN_DPM} (default 4.2V), the charge current limit is reduced down to prevent the further drop of the supply. When the IC enters this mode, the charge current is lower than the set value and the DPM_STATUS bit is set. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change. Figure 7 shows the VIN-DPM behavior to a current limited source. In this figure the input source has a 750mA current limit and the device charge current is increased until the input current limit of the adapter is reached and the supply collapses. If the 2X timer is set, the safety timer is extended while V_{IN}-DPM is active. Additionally, termination is disabled.

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Device Functional Modes (continued)

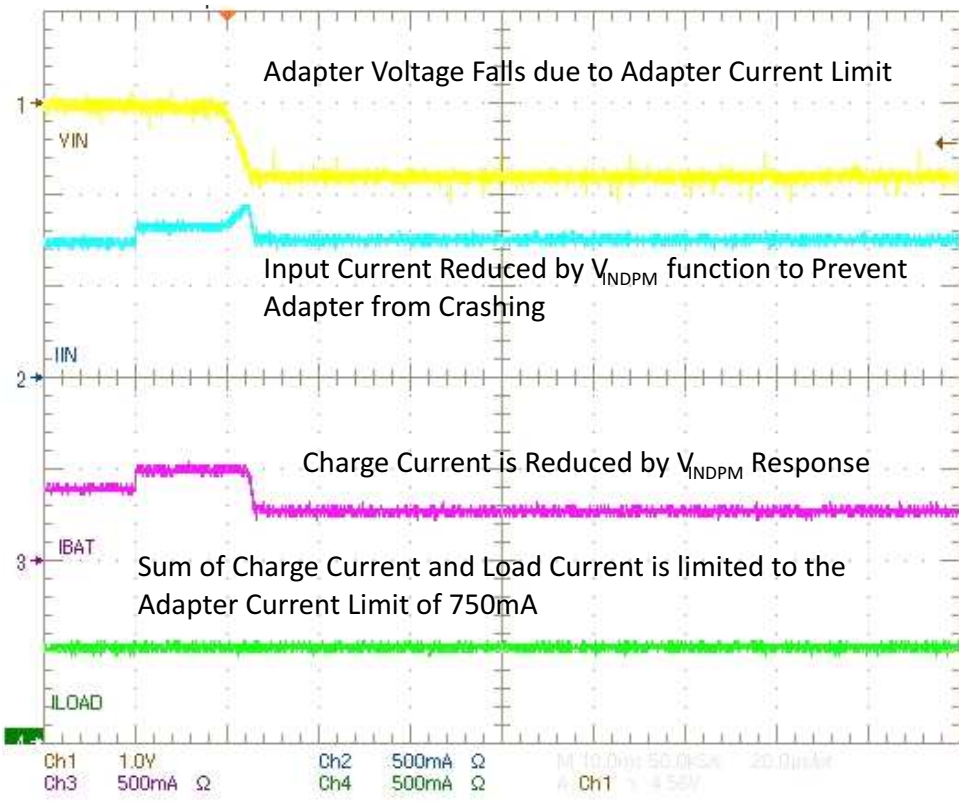


Figure 7. bq24187 V_{INDPM}

8.4.1.1.1.3 Input Over-Voltage Protection

The bq24187 provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from V_{IN} to PGND). When $V_{IN} > V_{OVP}$, the bq24187 turns off the PWM converter, sends a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I^2C. Once the OVP fault is removed, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

8.4.1.1.2 Charge Mode Operation

8.4.1.1.2.1 Charge Profile

When a valid input source is connected, the $\overline{CE}$ bit in the control register determines whether a charge cycle is initiated. By default, the bq24187 enables the charge cycle when a valid input source is connected ($V_{IN}>V_{UVLO}$ and $V_{BAT}+V_{SLP}<V_{IN}<V_{OVP}$). There are 4 loops that influence the charge current; constant current loop (CC), constant voltage loop (CV), thermal regulation loop and input voltage dynamic power management loop (V_{IN-DPM}). During the charging process, all four loops are enabled and the one that is dominant takes control. The bq24187 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. Figure 8 shows a typical charge.

Device Functional Modes (continued)

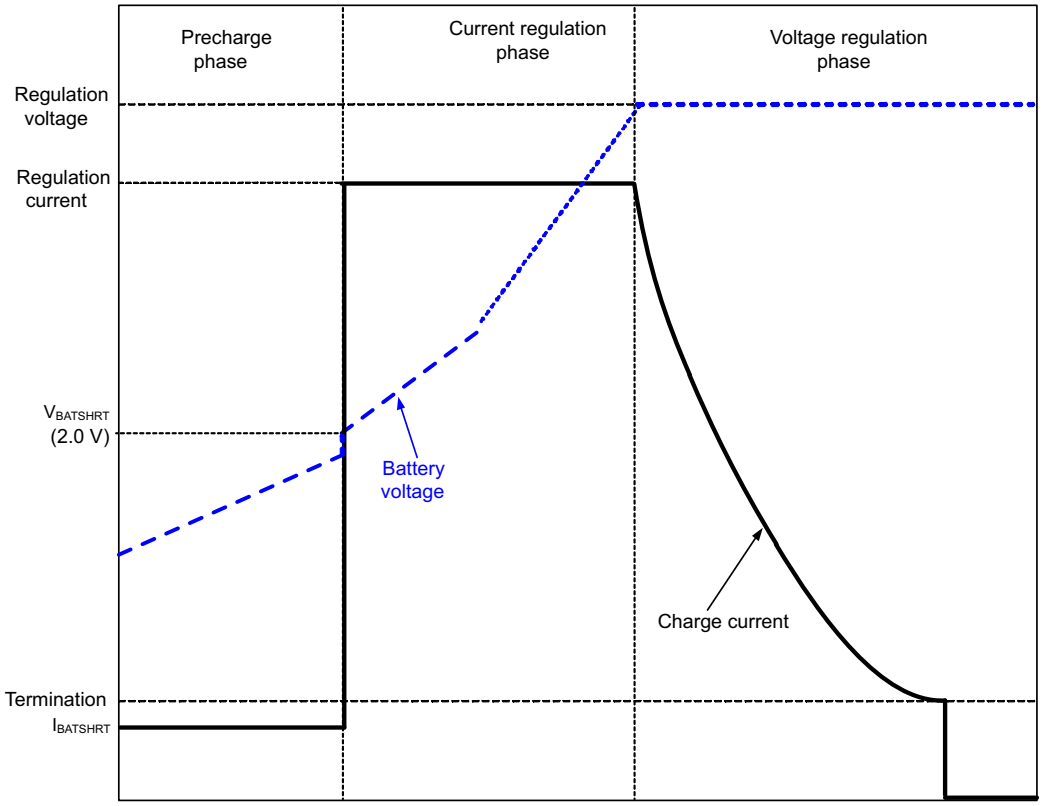


Figure 8. Typical Charging Profile Of Bq24187

8.4.1.1.3 Battery Charging Process

When the battery is deeply discharged or shorted, the bq24187 applies $I_{BATSHORT}$ to the battery to close the battery protector switch and bring the battery voltage up to acceptable charging levels. Once the battery rises above $V_{BATSHRT}$, the charge current is regulated to the value set in the I^2C register by the I_{CHARGE} bits. The charge current is regulated to I_{CHARGE} until the voltage between BAT and PGND reaches the regulation voltage. The voltage between BAT and PGND is regulated to VBATREG (CV mode) while the charge current naturally tapers down as shown in Figure 8. During the CC or CV modes, if the die temperature heats up, the thermal regulation loop reduces the input current to maintain a die temperature at 125°C.

When termination is enabled (TE bit is '1'), the bq24187 monitors the charging current during the CV mode. Once the charge current tapers down to the termination threshold, I_{TERM}, and the battery voltage is above the recharge threshold, the bq24187 terminates charge and enters battery detection (see Battery Detection section for more details). The termination current level is programmable. To disable the charge current termination, the host sets the charge termination bit (TE) of charge control register to 0. Refer to I^2C section for details. When termination is disabled, V_{BAT} is continuously regulated to V_{BATREG}. Termination is also disabled when any loop is active other than CC or CV. This includes V_{INDPM}, input current limit, or thermal regulation. Termination is also disabled during TS WARM/COOL conditions and when the LOW_CHG bit is set to '1'. A charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the V_{BATREG}-V_{RCH} threshold
- IN Power-on reset (POR)
- $\overline{CE}$ bit toggle or RESET bit is set (Host controlled)
- CD terminal is toggled

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Device Functional Modes (continued)

8.4.1.1.3.1 Charge Time Optimizer

The CC to CV transition is enhanced in the bq24187 architecture. The "knee" between CC and CV is very sharp. This enables the charger to remain in CC mode as long as possible before beginning to taper the charge current (CV mode). This provides a decrease in charge time as compared to older topologies.

8.4.1.1.4 Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from V_{BAT} for $t_{DETECT(SNK)}$ to verify there is a battery. If the battery voltage remains above V_{DETECT} for the full duration of $t_{DETECT(SNK)}$, a battery is determined to be present and the IC enters “Charge Done”. If V_{BAT} falls below V_{DETECT}, a “Battery Not Present” fault is signaled, the charge parameters are reset (V_{BATREG}, I_{CHARGE} and I_{TERM}) and battery detection continues. The next cycle of battery detection, the bq24187 turns on $I_{BATSHRT}$ for $t_{DETECT(SRC)}$. If V_{BAT} rises to $V_{DET(SRC1)}$, the current source is turned off and a “No Battery” condition is registered. In order to keep V_{BAT} high enough to close the battery protector, the current source turns on if V_{BAT} falls to $V_{DET(SRC2)}$. The source cycle continues for $t_{DETECT(SRC)}$. After $t_{DETECT(SRC)}$, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. Battery detection is not performed when termination is disabled.

8.4.1.1.5 Battery Overvoltage Protection (BOVP)

If the battery is ever above the battery OVP threshold (V_{BOVP}), the battery OVP circuit shuts the PWM converter off to discharge the battery to safe operating levels. A battery OVP most commonly occurs when the bq24187 returns to DEFAULT mode after a watchdog timer expiration or RESET bit written to '1'. In this condition, the V_{BATREG} is reset and may be below the battery voltage. Other conditions may be when the input is initially plugged in before I^2C communication is established or TS WARM conditions or when writing the VBATREG to less than the battery voltage. The battery OVP condition is cleared when the battery voltage falls below the hysteresis of V_{BOVP} either by the battery discharging or writing the V_{BATREG} to a higher value. When a battery OVP event exists for $t_{DGL(BOVP)}$, the bq24187 sends a single 128µs pulse on the STAT/ INT outputs and the STATx and FAULT_x bits are updated in the I2C. Once the BOVP fault is removed, the STATx bits are cleared and the device returns to normal operation. The FAULT_x bits are not cleared until they are read in the I2C after the BOVP condition no longer exists.

8.4.1.1.6 Default Mode

DEFAULT mode is used when I^2C communication is not available. DEFAULT mode is entered in the following situations:

1. When the charger is enabled before I^2C communication is established
2. When the watchdog timer expires without a reset from the I^2C interface
3. The RESET bit is written in the I^2C register

In DEFAULT mode, the I^2C registers are reset to the default values. The 1.25 min safety timer is reset and starts when DEFAULT mode is entered if a charge cycle is underway. The default value for V_{BATREG} is 3.6V, and the default value for I_{CHARGE} is 1A. The input current limit in DEFAULT mode is set by PSEL. (See *Power Source Selector Input* section) DEFAULT mode is exited by writing to the I^2C interface. Note that if termination is enabled and charging has terminated, a new charge cycle is NOT initiated when entering DEFAULT mode.

8.4.1.1.7 Power Source Selector Input (PSEL)

The bq24187 contains a PSEL input that is used to program the input current limit during DEFAULT mode. Drive PSEL high to indicate a USB source is connected to the input and program the 100mA current limit for IN. Drive PSEL low to indicate that an AC Adapter is connected to the input. When PSEL is low, the IC starts up with a 1.5A input current limit. Once an I^2C write is done and the device is in HOST mode, the PSEL has no effect on the input current limit until the watchdog timer expires and returns the bq24187 to DEFAULT mode.

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Device Functional Modes (continued)

8.4.1.1.8 Safety Timer and Watchdog Timer In Charge Mode

At the beginning of charging process, the bq24187 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the IC enters suspend mode where charging is disabled. The safety timer time is selectable using the I2C interface. When a safety timer fault occurs, a single 128µs pulse is sent on the STAT and INT outputs and the STATx bits of the status registers are updated in the I^2C. The $\overline{CE}$ bit, HZ_MODE bit, CD terminal or input power must be toggled in order to clear the safety timer fault. The safety timer duration is selectable using the TMR_X bits in the Safety Timer Register/ NTC Monitor register. Changing the safety timer duration resets the safety timer.

In addition to the safety timer, the bq24187 contains a 30-second ($t_{WATCHDOG}$) watchdog timer that monitors the host through the I^2C interface. Once a write is performed on the I^2C interface, a watchdog timer is started. The watchdog timer is reset by the host using the I2C interface. This is done by writing a “1” to the reset bit (TMR_RST) in the control register. The TMR_RST bit is automatically set to “0” when the watchdog timer is reset. This process continues until battery is fully charged or the safety timer expires. If the watchdog timer expires, the IC enters DEFAULT mode where the default charge parameters are loaded, the safety timer restarts at 1.25 minutes and charging continues. The I^2C may be accessed again to reinitialize the desired values and restart the watchdog timer as long as the safety timer has not expired. Once the safety timer expires, charging is disabled. This function prevents continuous charging of a defective battery if the host fails to reset the safety timer. In the event the watchdog timer expires, the I^2C circuit is reset as well. This prevents the I^2C from indefinitely hanging if the I^2C master loses control during a read/write. The watchdog timer flow chart is shown in Figure 9.

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Device Functional Modes (continued)

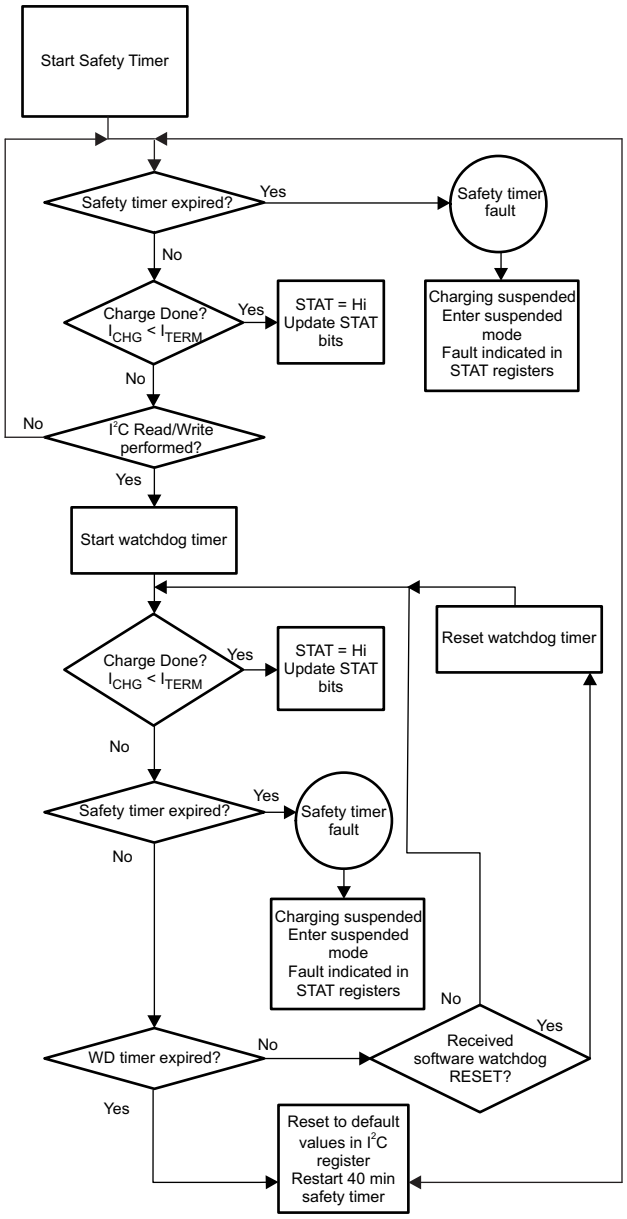


Figure 9. The Watchdog Timer Flow Chart For Bq24187

8.4.1.1.9 LDO Output (DRV)

The bq24187 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.3V so it ideal to protect voltage sensitive USB circuits. The LDO is on whenever a supply is connected to the input of the bq24187. The LDO is on whenever a supply is connected to the input of the bq24187. The DRV is disabled under the following conditions:

1. V_{SUPPLY} < UVLO
2. V_{SUPPLY} < V_{BAT} + V_{SLP}
3. Thermal Shutdown

Device Functional Modes (continued)

8.4.1.1.10 External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the bq24187 provides a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The JEITA specification is shown in Figure 10.

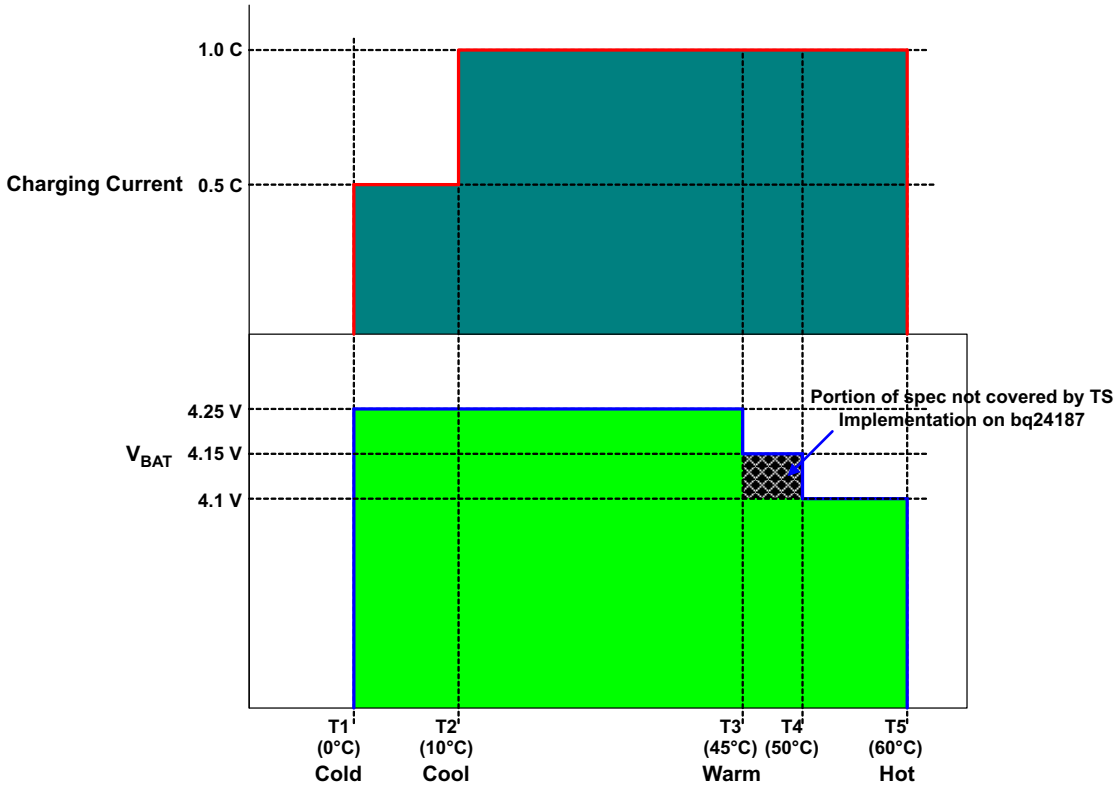


Figure 10. Charge Current During TS Conditions

To satisfy the JEITA requirements, four temperature thresholds are monitored; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C) and the hot battery threshold (T_{NTC} > 60°C). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds in the EC table. Charging is suspended and timers are suspended when V_{TS} < V_{HOT} or V_{TS} > V_{COLD}. When V_{COOL} < V_{TS} < V_{COLD}, the charging current is reduced to half of the programmed charge current. When V_{HOT} < V_{TS} < V_{WARM}, the battery regulation voltage is reduced by 140mV from the programmed regulation threshold. The TS function is disabled by connecting TS directly to DRV (V_{TS} > V_{TSOFF}).

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 11. The resistor values are calculated using the following equations:

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (1)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (2)$$

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Device Functional Modes (continued)

Where:

$V_{COLD} = 0.60 \times V_{DRV}$

$V_{HOT} = 0.30 \times V_{DRV}$

$$RCOOL = \frac{RLO \times RHI \times 0.564}{RLO - RLO \times 0.564 - RHI \times 0.564} \quad (3)$$

$$RWARM = \frac{RLO \times RHI \times 0.383}{RLO - RLO \times 0.383 - RHI \times 0.383} \quad (4)$$

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

The WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using Equation 3 and Equation 4.

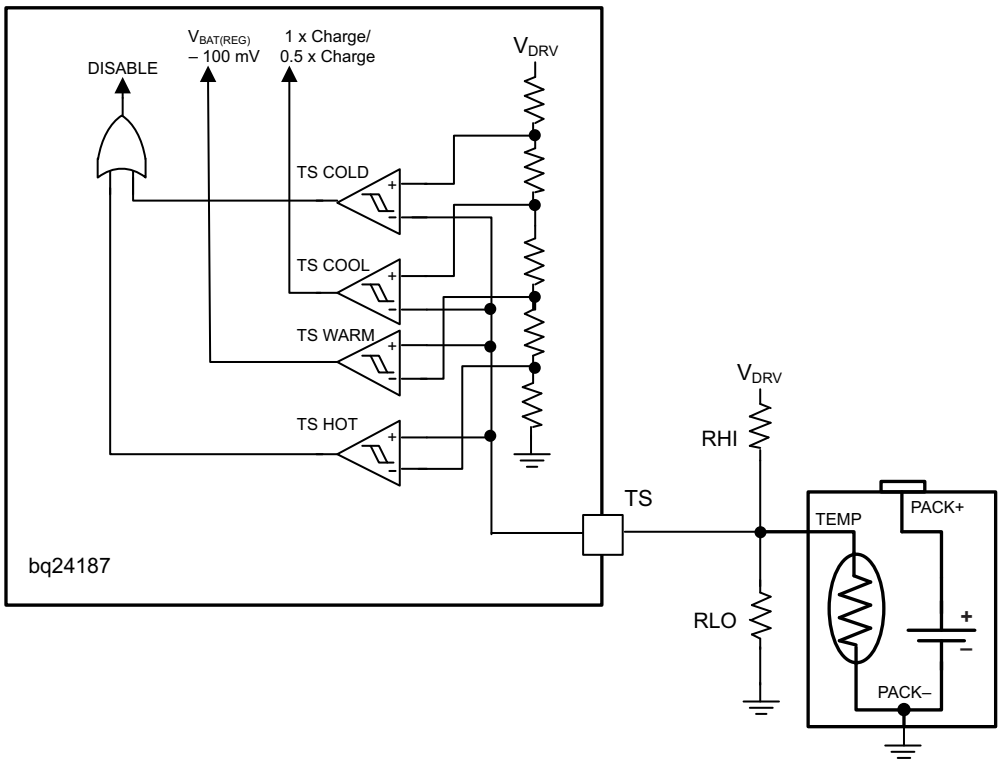


Figure 11. TS Circuit

8.4.1.1.11 Thermal Regulation and Protection

During the charging process, to prevent overheating in the chip, bq24187 monitors the junction temperature, T_J, of the die and reduces the input current once T_J reaches the thermal regulation threshold, T_{REG}. The input current is reduced to zero when the junction temperature increases about 10°C above T_{REG}. Once the input current is reduced to 0, the system current is reduced while the battery supplements the load to supply the system. When the input current is completely reduced to 0 and T_J>125°C, this is may cause a thermal shutdown of the bq24187 if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, bq24187 stops charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, all timers are suspended, and a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. The charge cycle resumes when T_J falls below T_{SHTDWN} by approximately 10°C.

Device Functional Modes (continued)

8.4.1.1.12 Charge Status Outputs (STAT, INT)

The STAT/INT output is used to indicate operation conditions for bq24187. STAT/INT is pulled low during charging when EN_STAT bit in the control register is set to “1”. When charge is complete or disabled, STAT/INT is high impedance. When a fault occurs, a 128-µs pulse (interrupt) is sent out to notify the host. The status of STAT/INT during different operation conditions is summarized in Table 1. STAT/INT drives an LED for visual indication or can be connected to the logic rail for host communication. The EN_STAT bit in the control register is used to enable/disable the charge status for STAT/INT. The interrupt pulses are unaffected by EN_STAT and will always be shown.

Table 1. STAT Terminal Summary

CHARGE STATE	STAT
Charge in progress and EN_STAT=1	Low
Other normal conditions	High-Impedance
Charge mode faults: Timer fault, sleep mode, VIN over voltage, VIN < UVLO, thermal shutdown	128-µs pulse, then High Impedance

8.4.2 Boost Mode Operation

In HOST mode, when the operation mode bit (BOOST_EN) in the control register (bit 6 in register 0x00h) is set to 1, bq24187 operates in boost mode and delivers 5V to IN to supply USB OTG devices connected to the USB connector. Boost operation can start with VBAT between 3.45V to 4.5V, and will maintain boost output until VBAT falls to 3.3V. IN supplies up to 1A to power these devices. It is not recommended to operate boost mode when the battery voltage is less than 3.3V. Proper operation is **not** guaranteed.

8.4.2.1 PWM Controller In Boost Mode

Similar to charge mode operation, in boost mode the IC switches at 1.5MHz to regulate the voltage at IN to 5V. The voltage control loop is internally compensated to provide enough phase margin for stable operation with the full battery voltage range and up to 750mA.

In boost mode, the cycle-by-cycle current limit is set to 4A or 2A (depending on the I^2C setting) to provide protection against short circuit conditions. If the cycle-by-cycle current limit is active for 8 ms, an overload condition is detected and the device exits boost mode, and signals an over-current fault. Additionally, discharge current limit ($I_{LIM(DISCH)}$) is active to protect the battery from overload. Synchronous operation and burst mode are used to maximize efficiency over the full load range.

The bq24187 will not enter boost mode unless the IN voltage is less than the UVLO and the IC is in high impedance mode. When the boost function is enabled, the bq24187 enters a linear mode to bring IN up to the battery voltage. Once $V_{IN} > (V_{BAT} – 1V)$, the bq24187 begins switching and regulates IN up to 5V. If V_{IN} does not rise to within 1V of V_{BAT} within 8ms, an over-current event is detected and boost mode is exited and a boost mode over-current event is announced, the BOOST bit is reset to ‘0’ and the STAT_x and FAULT_x bits in the Status/ Control register are updated.

8.4.2.2 Burst Mode During Light Load

In boost mode, the IC operates using burst mode to improve light load efficiency and reduce power loss. During boost mode, the PWM converter is turned off when the devices reaches minimum duty cycle and the output voltage rises to V_{BURST_ENT} threshold. This corresponds to approximately a 75mA inductor current. The converter then restarts when V_{IN} falls to V_{BURST_EXT}. See Figure 21 in the Application Curves for an example waveform.

8.4.2.3 Watchdog Timer In Boost Mode

During boost mode, the watchdog timer is active. The watchdog timer works the same as in charge mode. Write a “1” to the TMR_RST reset bit in the control register. If the watchdog timer expires, the IC resets the BOOST bit to 0, signals the fault pulse on the STAT and INT terminals and sets fault status bits in the status register.

8.4.2.4 STAT/ INT During Boost Mode

During boost mode, the STAT and INT outputs are high impedance. Under fault conditions, a 128µs pulse is sent out to notify the host of the error condition.

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8.4.2.5 Protection In Boost Mode

8.4.2.5.1 Output Over-Voltage Protection

The bq24187 contains integrated over-voltage protection on the IN terminal. During boost mode, if an over-voltage condition is detected (V_{IN}.$V_{BOOSTOVP}$), the IC turns off the PWM converter, resets EN_BOOST bit to 0, sets fault status bits and sends out a fault pulse on STAT and INT. The converter does not restart when VIN drops to the normal level until the EN_BOOST bit is reset to 1.

8.4.2.5.2 Output Over-Current Protection

The bq24187 contains over current protection to prevent the device and battery damage when IN is overloaded. When an over-current condition occurs, the cycle-by-cycle current limit limits the current from the battery to the load. If the overload condition lasts for 8 consecutive cycles, the overload fault is detected. When an overload condition is detected, the bq24187 turns off the PWM converter, resets BOOST bit to 0, sets the fault status bits and sends out the fault pulse on STAT and INT. The boost starts only after the fault is cleared and the EN_BOOST bit is reset to 1 using the I^2C.

8.4.2.5.3 Battery Overvoltage Protection

During boost mode, when the battery voltage is below the minimum battery voltage threshold, VBATUVLO, the IC turns off the PWM converter, resets BOOST bit to 0, sets fault status bits and sends out a fault pulse on STAT and INT. Once the battery voltage returns to the acceptable level, the boost starts after the BOOST bit is set to 1. Proper operation below 3.3V down to the $V_{BATUVLO}$ is not specified.

8.5 Programming

8.5.1 Serial Interface Description

The bq24187 uses an I^2C compatible interface to program charge parameters. I^2C™ is a 2-wire serial interface developed by Philips Semiconductor (see I2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O terminals, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The bq24187 device works as a slave and supports the following data transfer modes, as defined in the I^2C Bus™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as battery voltage remains above 2.5 V (typical). The I^2C circuitry is powered from VBUS when a supply is connected. If the VBUS supply is not connected, the I^2C circuitry is powered from the battery through CSOUT. The battery voltage must stay above 2.5V with no input connected in order to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The bq24187/1 device only supports 7-bit addressing. The device 7-bit address is defined as ‘1101011’ (0x6Bh).

8.5.1.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 12. All I^2C-compatible devices should recognize a start condition.

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Programming (continued)

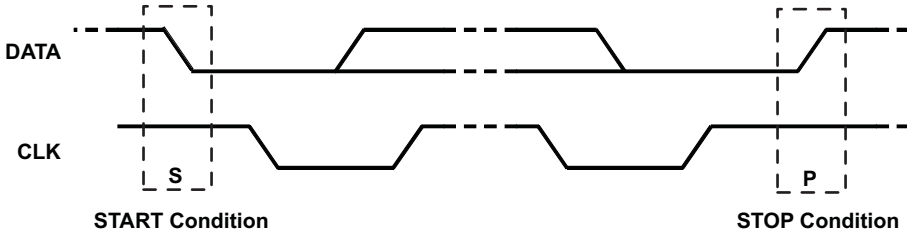


Figure 12. Start And Stop Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 13). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 13) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

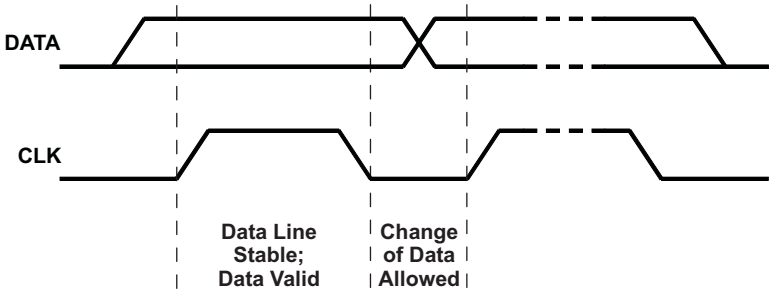


Figure 13. Bit Transfer On The Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 15). This releases the bus and stops the communication link with the addressed slave. All I2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I2C logic from getting stuck in a bad state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

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Programming (continued)

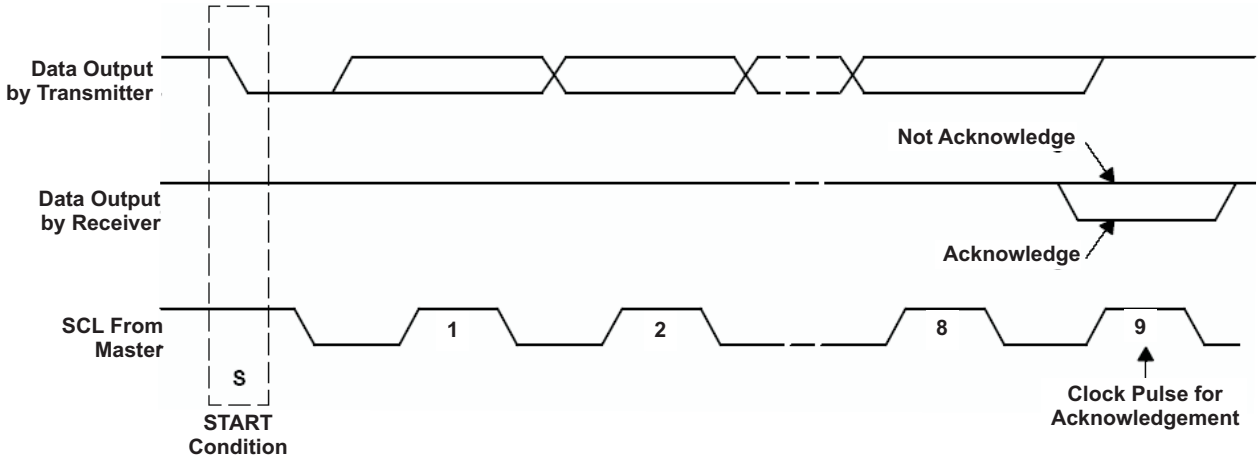


Figure 14. Acknowledge On The I²C Bus

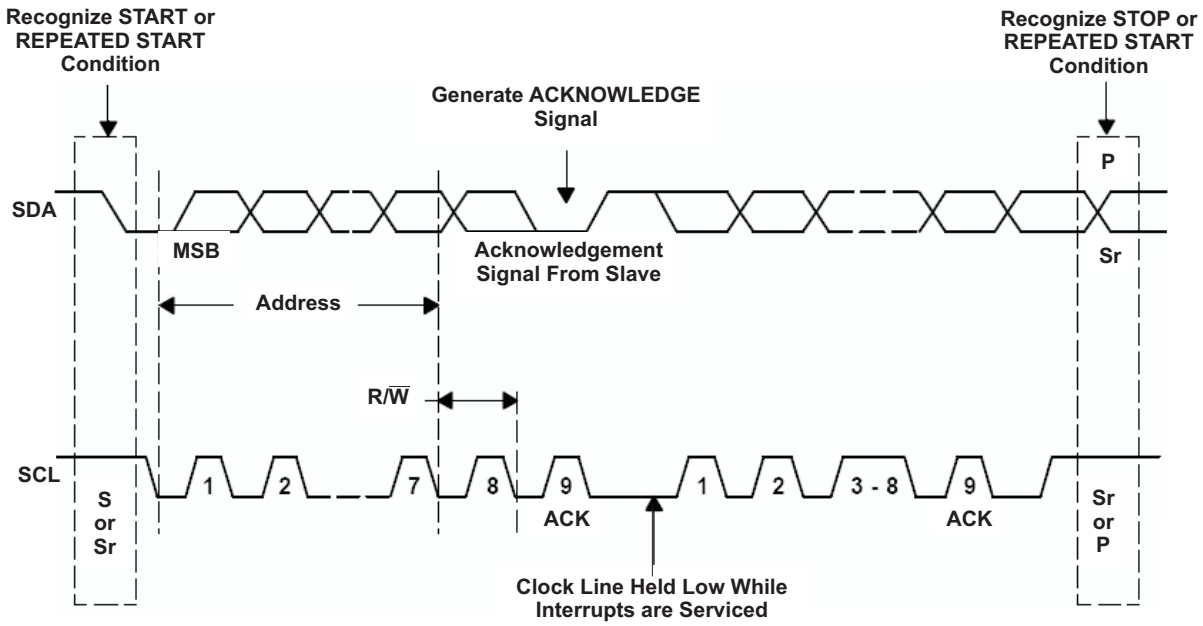


Figure 15. Bus Protocol

8.6 Register Maps

Table 2. Status/Control Register (READ/WRITE)
Memory Location: 00, Reset State: 00xx 0xxx

BIT	NAME(1) (2)	READ/WRITE	FUNCTION
B7 (MSB)	TMR_RST	Read/Write	Write: TMR_RST function, write "1" to reset the watchdog timer (auto clear) Read: Always 0
B	BOOST	Read/Write	0-Charger Mode 1-Boost Mode (default 0)
B5	STAT_1	Read Only	00-Ready 01-Charge in progress, 10-Charge done 11-Fault
B4	STAT_0	Read Only	
B3	NA	Read/Write Only	NA
B2	FAULT_2	Read Only	000-Normal 001-V_{IN} > V_{OVP} or Boost Mode OVP 010- Low Supply connected (V_{IN}<V_{UVLO} or V_{IN}<VS_{LP}) or Boost Mode Overcurrent 011- Thermal Shutdown 100-Battery Temperature Fault 101- Timer Fault (watchdog or safety timer) 110-Battery OVP 111-No Battery connected
B1	FAULT_1	Read Only	
B0 (LSB)	FAULT_0	Read Only	

(1) STAT_x bits show current status. These bits change based on the current condition.
(2) FAULT_x bits show faults. If a fault occurs, these bits announce the fault and do not clear until read. If more than one fault occurs, the first fault is shown.

BOOST Bit (Operation Mode)

The BOOST bit selects the operation mode for the bq24187. Write a “1” to enable boost mode and regulate IN to 5V to supply OTG peripherals. See “Boost Mode Operation” section for more details

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Table 3. Control Register (Read/Write)
Memory Location: 01, Reset State: 1xxx 1110

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	RESET	Write only	Write: 1-Reset all registers to default values 0-No effect Read: always get “1”
B6	IN_LIMIT_2	Read/Write	000-USB2.0 host with 100mA current limit 001-USB3.0 host with 150mA current limit 010 – USB2.0 host with 500mA current limit 011 – USB3.0 host/charger with 900mA current limit 100 – Charger with 1500mA current limit 101—NA 110 – Charger with 2500mA current limit 111-NA (default xxx(1))
B5	IN_LIMIT_1	Read/Write	
B4	IN_LIMIT_0	Read/Write	
B3	EN_STAT	Read/Write	0-Disable STAT function (STAT only shows faults) 1-Enable STAT function (default 1)
B2	TE	Read/Write	0-Disable charge current termination 1-Enable charge current termination (default 1)
B1	$\overline{CE}$	Read/Write	0-Charger enabled 1-Charger is disabled (default 0)
B0 (LSB)	HZ_MODE	Read/Write	0-Not high impedance mode 1-High impedance mode (default 0)

(1) When in DEFAULT mode, the D+/D– inputs or PSEL determine the default input current limit.

RESET Bit

The RESET bit in the control register (0x01h) is used to reset all the charge parameters. Write “1” to RESET bit to reset all the registers to default values and place the bq24187 into DEFAULT mode and turn off the watchdog timer. The RESET bit is automatically cleared to zero once the bq24187 enters DEFAULT mode.

$\overline{CE}$ Bit (Charge Enable)

The $\overline{CE}$ bit in the control register (0x01h) is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge.

HZ_MODE Bit (High Impedance Mode Enable)

The HZ_MODE bit in the control register (0x01h) is used to disable or enable the high impedance mode. A low logic level (0) on this bit enables the IC and a high logic level (1) puts the IC in a low quiescent current state called high impedance mode. When in high impedance mode, the converter is off.

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Table 4. Control/Battery Voltage Register (Read/Write)
Memory Location: 02, Reset State: 0001 0100

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	V_{BREG5}	Read/Write	Battery Regulation Voltage: 640 mV (default 0)
B6	V_{BREG4}	Read/Write	Battery Regulation Voltage: 320 mV (default 0)
B5	V_{BREG3}	Read/Write	Battery Regulation Voltage: 160 mV (default 0)
B4	V_{BREG2}	Read/Write	Battery Regulation Voltage: 80 mV (default 0)
B3	V_{BREG1}	Read/Write	Battery Regulation Voltage: 40 mV (default 1)
B2	V_{BREG0}	Read/Write	Battery Regulation Voltage: 20 mV (default 0)
B1	MOD_FREQ1	Read/Write	Modify Switching Frequency Target – 00 – No Change to Nominal Frequency Target 01 – +10% Change to Nominal Frequency 10 – –10% Change to Nominal Frequency 11 – NA (default 00)
B0 (LSB)	MOD_FREQ2	Read/Write	

V_{BREG} Bits (Battery Regulation Threshold setting)

Use V_{BREG} bits to set the battery regulation threshold. The VBATREG is calculated using the following equation:

$V_{BATREG} = 3.5\ V + V_{BREG}CODE \times 20\ mV$

The charge voltage range is 3.5V to 4.44V with the offset of 3.5V and step of 20mV. The default setting is 3.6V. If a value greater than 4.44V is written, the setting goes to 4.44V. It is recommended to set V_{BATREG} above V_{MINSYS}.

MOD_FREQx Bits (Frequency Modification)

The MOD_FREQx bits are used to change the switching frequency by ±10%. This is used for applications where the 1.5MHz switching frequency noise interferes with other device operation. The frequency may be modified by ±10% of the nominal frequency.

Table 5. Vender/Part/Revision Register (Read only)
Memory Location: 03, Reset State: 0100 0110

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	Vender2	Read Only	Vender Code: bit 2 (default 0)
B6	Vender1	Read Only	Vender Code: bit 1 (default 1)
B5	Vender0	Read Only	Vender Code: bit 0 (default 0)
B4	PN1	Read Only	For I^2C Address 6Bh: 00–bq24187
B3	PN0	Read Only	
B2	Revision2	Read Only	Revision Code
B1	Revision1	Read Only	
B0 (LSB)	Revision0	Read Only	

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Table 6. Battery Termination/Fast Charge Current Register (Read/Write)
Memory Location: 04, Reset State: 0010 1010

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	V_{ICHRG4}	Read/Write	Charge current: 1600mA – (default 0)
B6	V_{ICHRG3}	Read/Write	Charge current: 800mA— (default 0)
B5	V_{ICHRG2}	Read/Write	Charge current: 400mA—(default 1)
B4	V_{ICHRG1}	Read/Write	Charge current: 200mA— (default 0)
B3	V_{ICHRG0}	Read/Write	Charge current: 100mA (default 1)
B2	V_{ITERM2}	Read/Write	Termination current sense: 200mA (default 0)
B1	V_{ITERM1}	Read/Write	Termination current sense voltage: 100mA (default 1)
B0 (LSB)	V_{ITERM0}	Read/Write	Termination current sense voltage: 50mA (default 0)

I_{CHRG} Bits (Charge Current Regulation Threshold setting)

Use I_{CHRG} bits to set the charge current regulation threshold. The charge current is programmable from 500mA to 2A in 100mA steps. The default is 1A. The I_{CHARGE} is calculated using the following equation:
I_{CHARGE} = 500 mA + I_{CHRG}CODE× 50 mA

ITERM Bits (Charge Current Termination Threshold setting)

Use I_{TERM} bits to set the charge current termination threshold. The termination threshold is programmable from 50mA to 300mA in 50mA steps. The default is 150mA. The I_{TERM} is calculated using the following equation:
I_{TERM} = 50 mA + I_{TERM}CODE × 50 mA
Any setting programmed above 300mA selects the 300mA setting.

Table 7. V_{IN-DPM} Voltage/ DPPM Status Register
Memory location: 05, Reset state: xx00 x000

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	NA	Read Only	NA
B6	DPM_STATUS	Read Only	0 – V_{IN}-DPM mode is not active 1 – V_{IN}-DPM mode is active
B5	LOW_CHG	Read/Write	0 – Normal charge current set by 04h 1 – Low charge current setting 300mA (default 0)
B4	NA	Read Only	NA
B3	CD_STATUS	Read Only	0 – CD low, IC enabled 1 – CD high, IC disabled
B2	V_{INDPM2}	Read/Write	Input V_{IN-DPM} voltage: V_{DPMOFF} + 8% (default 0)
B1	V_{INDPM1}	Read/Write	Input V_{IN-DPM} voltage: V_{DPMOFF} + 4% (default 0)
B0 (LSB)	V_{INDPM0}	Read/Write	Input V_{IN-DPM} voltage: V_{DPMOFF} + 2% (default 0)

V_{IN-DPM} voltage offset is 4.2V.

LOW_CHG Bit (Low Charge Mode Enable)

The LOW_CHG bit is used to reduce the charge current to a minimum current. This feature is used by systems where battery NTC is monitored by the host and requires a reduced charge current setting or by systems that need a “preconditioning” current for low battery voltages. Write a “1” to this bit to charge at 300mA. Write a “0” to this bit to charge at the programmed charge current.

V_{INDPM} Bits (VINDPM Threshold setting)

Use V_{INDPM} bits to set the V_{INDPM} regulation threshold. The V_{INDPM} threshold is calculated using the following equation:
V_{INDPM} = V_{INDPM_OFF} + V_{INDPM}CODE × 2% ×V_{INDPM_OFF}

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Table 8. Safety Timer/ NTC Monitor Register (READ/WRITE)
Memory location: 06, Reset state: 1001 1xx0

BIT	NAME	READ/WRITE	FUNCTION
B7 (MSB)	2XTMR_EN	Read/Write	0 – Timer not slowed at any time 1 – Timer slowed by 2x when in thermal regulation, V_{IN_DPM} or DPPM (default 1)
B6	TMR_1	Read/Write	Safety Timer Time Limit – 00—40 minute fast charge 01 – 6 hour fast charge 10 – 9 hour fast charge 11 – Disable safety timers (default 00) (bq24187/1 only)
B5	TMR_2	Read/Write	
B4	BOOST_ILIM	Read/Write	0—500mA 1—750mA (Default 1)
B3	TS_EN	Read/Write	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_FAULT1	Read only	TS Fault Mode: 00— Normal, No TS fault 01— TS temp < TC_{OLD} or TS temp > T_{HOT}(Charging suspended) 10— T_{COOL} > TS temp > T_{COLD} (Charge current reduced by half) 11— T_{WARM} < TS temp < T_{HOT} (Charge voltage reduced by 100mV)
B1	TS_FAULT0	Read only	
B0 (LSB)	NA	Read/Write	Always write to ‘0’

BOOST_ILIM Bit .(Boost current limit setting)

The BOOST_ILIM bit programs the cycle by cycle current limit threshold for boost operation. The 1A setting sets the low side cycle by cycle current limit to 4A (typ). This ensures that at least 1A can be supplied from the boost converter over the entire battery range. The 500mA setting sets the current limit to 2A(typ) to ensure at least 500mA available from the boost converter. See the boost mode over-current section for more details

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9 Applications and Implementation

9.1 Application Information

The bq24187-625 evaluation module (EVM) is a complete charger module for evaluating the bq24187. The application curves were taken using the bq24187EVM-625. See Related Documentation.

9.2 Typical Application

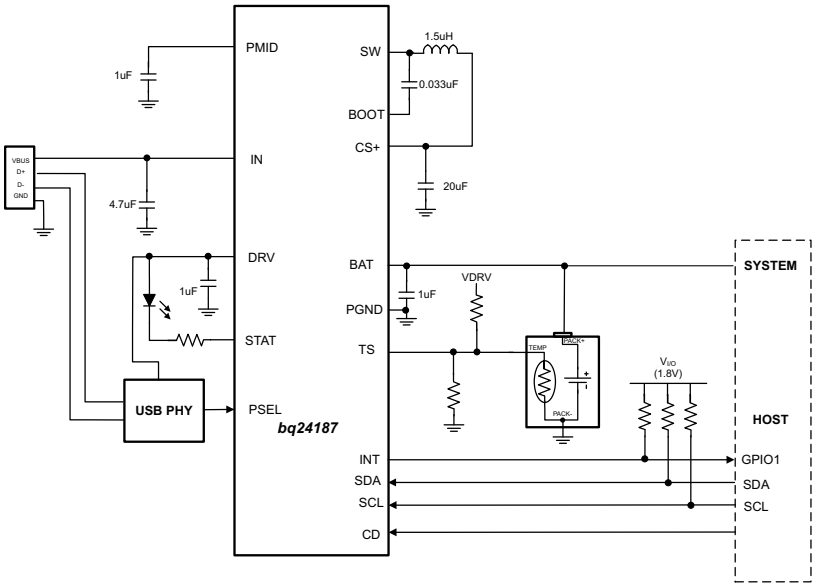


Figure 16. bq24187 Typical Application Circuit

9.2.1 Design Requirements

Table 9. Design Requirements

DESIGN PARAMATER	EXAMPLE VALUE
Input Voltage Range	4.75 V to 5.25 V nominal, withstand 28 V
Input Current Limit	1500 mA
Input DPM Threshold	4.25 V
Fast Charge Current	2000 mA
Battery Charge Voltage	4.2 V
Termination Current	150 mA

9.2.2 Detailed Design Procedure

The parameters are configurable using the EVM software.

The typical application circuit shows the minimum capacitance requirements for each terminal. Options for sizing the inductor outside the 1.5 µH recommended value and additional SYS terminal capacitance are explained in the next section. The resistors on STAT and INT are sized per each LED's current requirements. The TS resistor divider for configuring the TS function to work with the battery's specific thermistor can be computed from Equation 1 and Equation 2. The external battery FET is optional.

9.2.2.1 Output Inductor And Capacitor Selection Guidelines

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq24187 is designed to work with 1.5µH to 2.2µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.

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Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use Equation 5 and Equation 6 to calculate the peak current.

$$\%_{RIPPLE} = \frac{V_{IN} - V_{BAT}}{L} \times \frac{V_{BAT}}{V_{IN} \times f_{SW}} \quad (5)$$

For the 5V adapter case, a good rule of thumb is to use 3.5V as V_{BAT}. This provides a reasonable worst case ripple. For higher adapters, the closer to 50% duty cycle, the worse the ripple.

$$I_{PEAK} = I_{CHARGE} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (6)$$

The inductor selected must have a saturation current rating greater than or equal to the calculated I_{PEAK}. Due to the high currents possible with the bq24187, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$$I_{TEMPRISE} = I_{LOAD} + D \times (I_{PEAK} - I_{LOAD}) = 1.5A + 0.2 \times (2.5A - 1.5A) = 1.7A \quad (7)$$

The internal loop compensation of the bq24187 is designed to be stable with 10µF to 150µF of local capacitance but requires at least 20µF total capacitance on CS+. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 20µF and 47µF is recommended for local bypass to CS+. If more than 100µF is placed on CS+, place at least 10µF from BAT to GND.

9.2.3 Application Curves

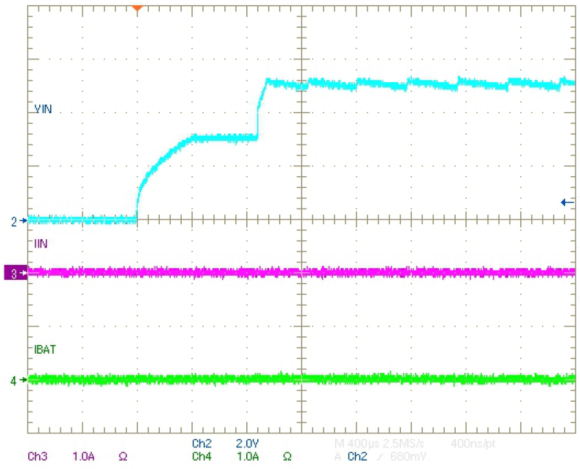


Figure 17. Boost Startup No Load

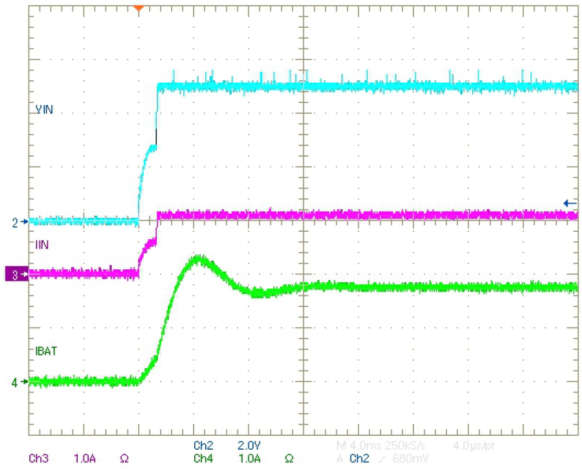


Figure 18. Boost Startup 1A Load

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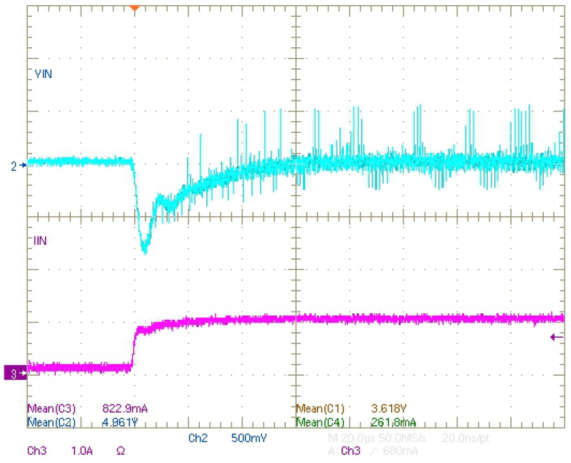


Figure 19. Boost Transient Response

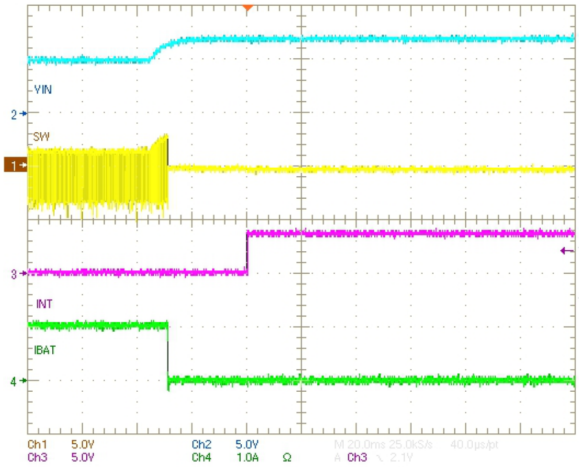


Figure 20. Input OVP Event With INT

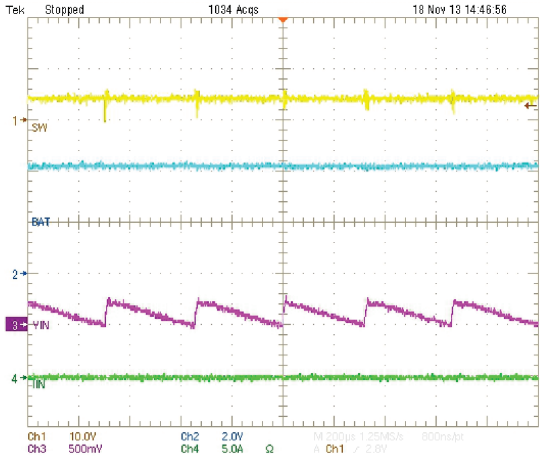


Figure 21. Boost Burst Mode During Light Load

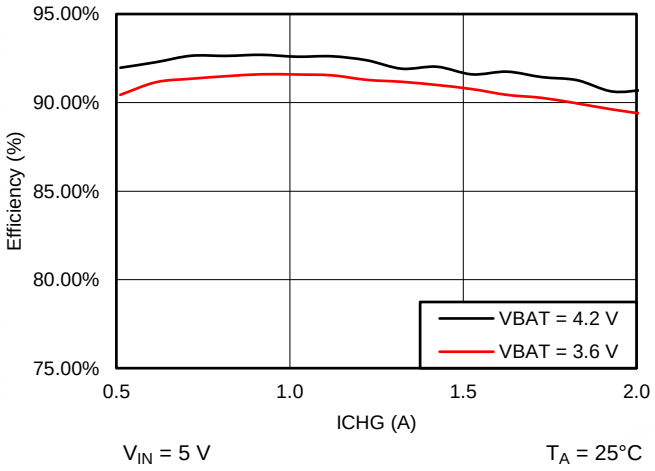


Figure 22. Charger Efficiency vs Battery Voltage

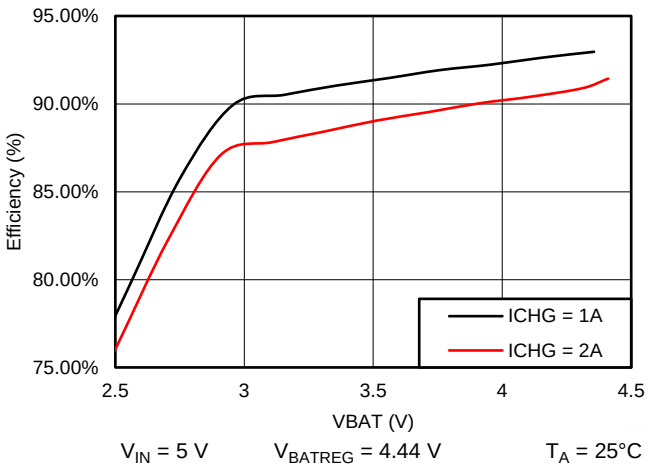


Figure 23. Charger Efficiency vs Charge Current

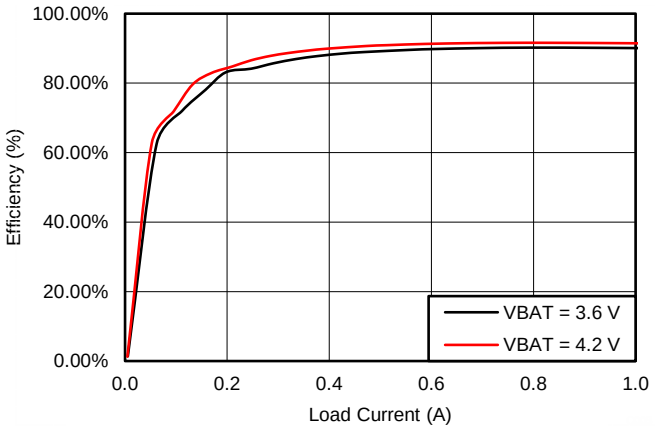


Figure 24. Boost Efficiency vs Load Current

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10 Layout

10.1 Layout Guidelines

It is important to pay special attention to the PCB layout. Figure 25 provides a sample layout for the high current paths of the bq24187YFF.

The following provides some guidelines:

- Place 4.7µF input capacitor as close to IN terminal and PGND terminal as possible to make high frequency current loop area as small as possible.
- Place 1µF input capacitor as close to PMID terminal and PGND terminal as possible to make high frequency current loop area as small as possible. Connect the GND of the PMID and IN caps as close as possible.
- The local bypass capacitor from CS+ to GND should be connected between the CS+ terminal and PGND of the IC. The intent is to minimize the current path loop area from the SW terminal through the LC filter and back to the PGND terminal.
- Place all decoupling capacitor close to their respective IC terminal and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into IN, BAT, CS+ and from the SW terminals must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND terminals should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

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10.2 Layout Example

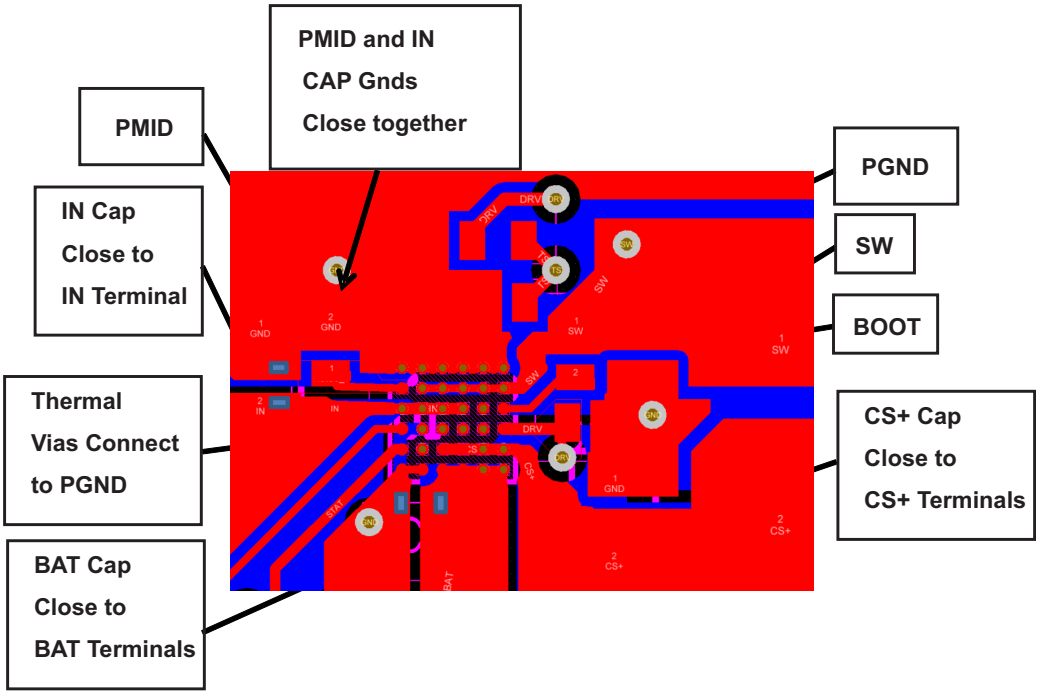


Figure 25. Recommended bq24187 PCB Layout For WCSP Package

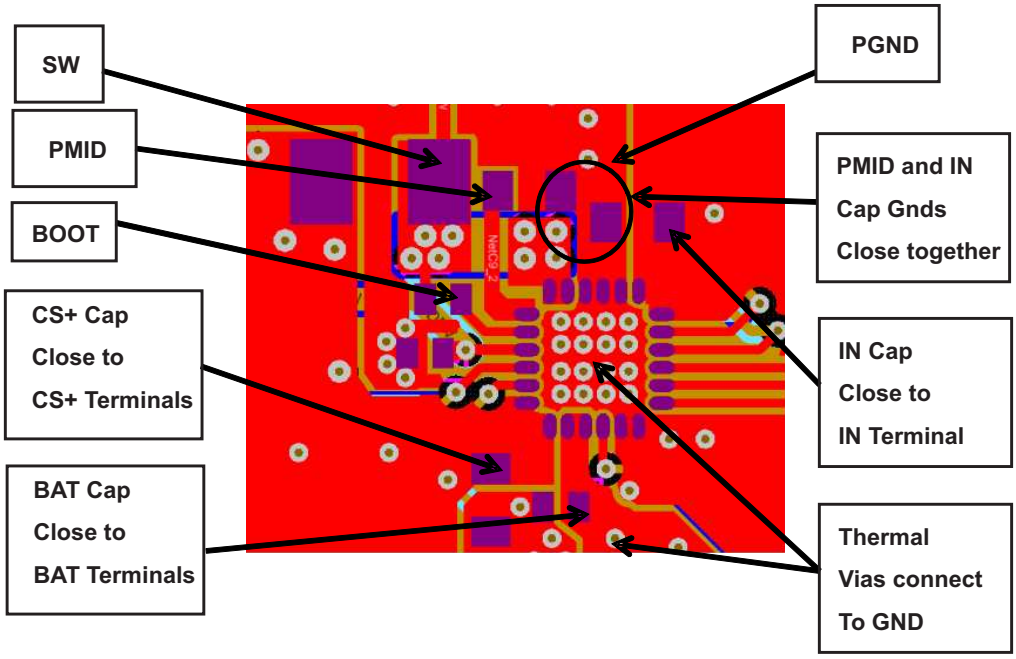


Figure 26. Recommended bq24187 PCB Layout For QFN Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

High-efficiency, Switch-mode Battery Charge Evaluation Module User's Guide, SLUUAI5

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24187YFFR	NRND	DSBGA	YFF	36	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24187	
BQ24187YFFT	NRND	DSBGA	YFF	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24187	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

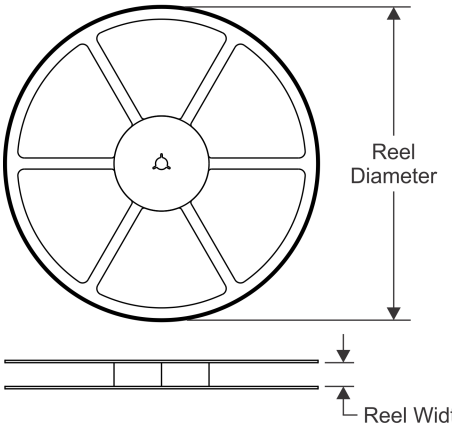
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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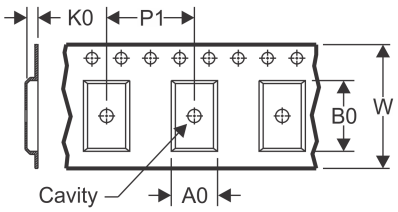
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

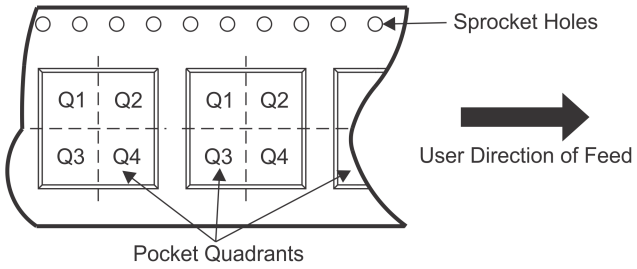


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

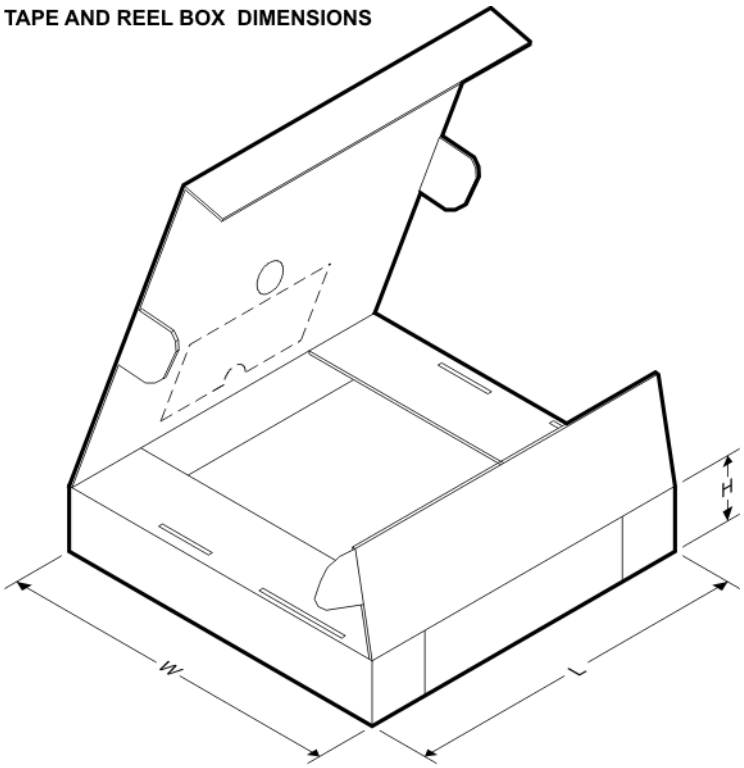
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24187YFFR	DSBGA	YFF	36	3000	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1
BQ24187YFFT	DSBGA	YFF	36	250	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

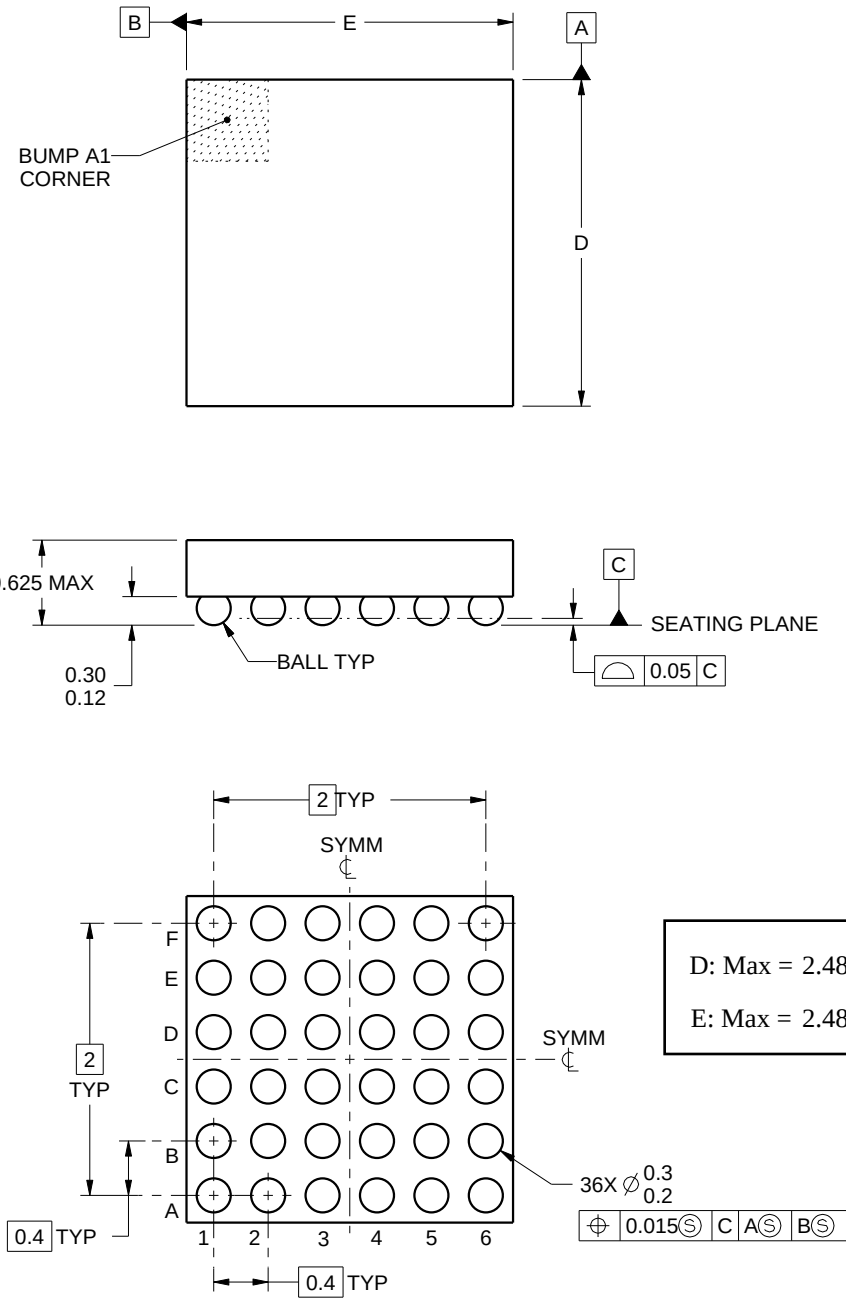
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24187YFFR	DSBGA	YFF	36	3000	182.0	182.0	20.0
BQ24187YFFT	DSBGA	YFF	36	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0036

DSBGA - 0.625 mm max height

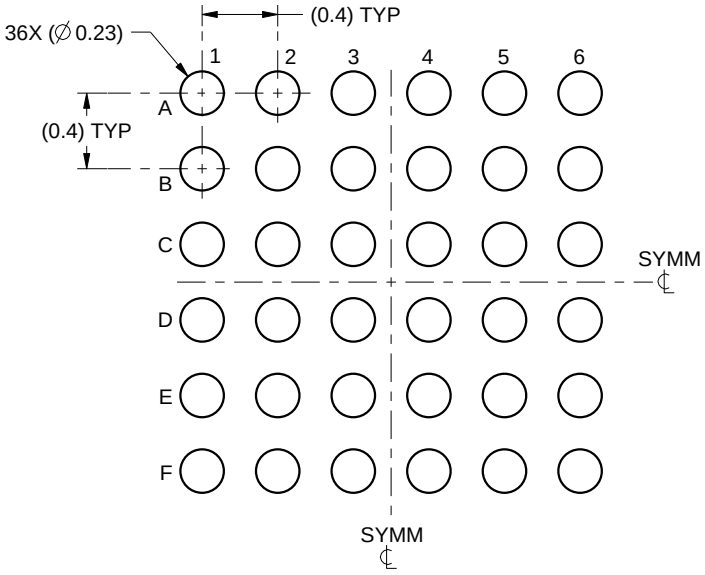
DIE SIZE BALL GRID ARRAY



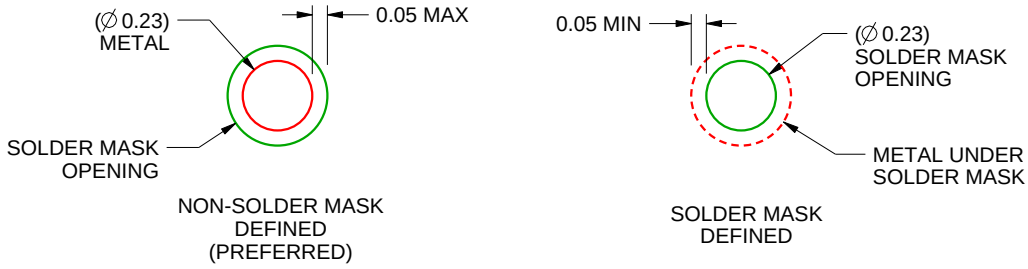
4222008/A 03/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X

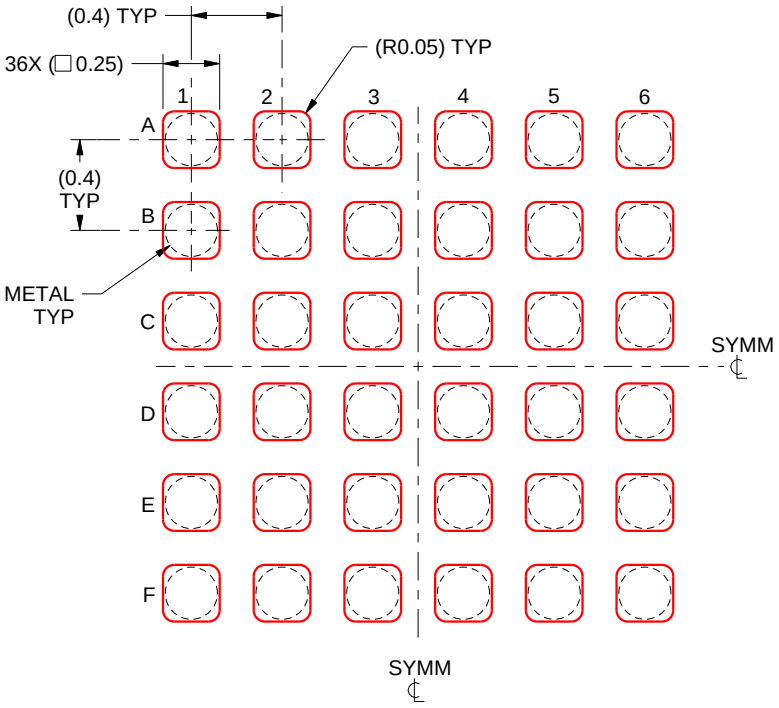


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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